Analysis on the Effectiveness of Clock Trace Termination Methods and Trace Lengths on a Printed Circuit Board

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ABSTRACT

To analyze the effectiveness of various termination methods for clock traces related to signal functionality based on routed trace lengths and edge rates. The following is examined:

1. Effectiveness of termination methods which provides optimal performance for a given application;
2. Efficient termination technique for preventing ringing, overshoot and reflections;
3. Effects of various trace lengths based on clock edge rates;
4. Effects of dual (multiple) terminations

Results of this analysis are from measurements taken on a specially designed printed circuit board in the time domain. A companion paper, *Analysis on the Effectiveness of Image Planes Within a Printed Circuit Board* uses the same printed circuit board with radiated measurements in the frequency domain.

INTRODUCTION

A major concern in designing a printed circuit board lies in trace routing for high threat signals. These signals include clock traces, differential pairs, audio, video, alarm, reset, and similar signals. This paper evaluates clock trace termination methods on a printed circuit board (PCB). Clock traces and how they are routed have a significant impact on every electronic device, regardless of actual clock speed or sophistication of technology used. Practicing engineers need to understand fundamental concepts related to terminations that allow for optimal functionality of design and signal quality.

Most designers have a limited time to design and manufacture a product, including modeling and computer simulation. If a product has poor signal quality and fails functionality tests, rework is required based on limited knowledge of how terminations on a PCB works.

A PCB was designed for flexibility in analyzing different termination methods. A clock driver injects a signal down a trace to an active load. Use of active components present a realistic condition that would be observed on a real PCB, taking into consideration parasitics that exist within the trace and board. Four termination methods are investigated. Shunt jumpers are provided to change the length of the trace route. Trace lengths vary from 3 inches (electrically small for signal propagation; time for the signal to travel from source-to-load and load-to-source) to 18 inches (electrically long which allows ringing and reflections to exist). Additional programmable trace lengths include 8 inches and 13 inches, not investigated herein.

ANALYSIS OF TEST ENVIRONMENT

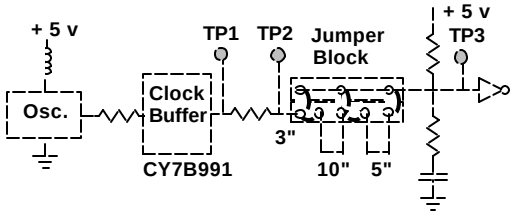
The following logic components were measured for actual edge rates and compared against the manufacturer's data sheet. It is observed that edge rates (rise time, T_{lh} and fall time, T_{hl}) differ significantly. Design engineers generally select devices based on functionality, propagation delay and published data, all for use in the time domain without considering the frequency domain aspects that components have using "actual" values.

Device	*Published* Edge Rate (ns) T_{lh}	T_{hl}	*Actual* Edge Rate (ns) T_{lh}	T_{hl}
74LS04	17-32	15-28	8.3	5.2
74HCT04	7-15	7-15	2.0	1.7
74ALS04	3-11	2-8	5.2	2.0
74F04	2.4-6.0	1.5-5.3	3.5	1.0
CY7B991	0.15-1.5	0.15-1.5	0.8	0.8

Table 1 Device Edge Rate Characteristics

0-78-3-5015-1/98/$10.00

To perform edge rate measurements, a high bandwidth digital signal analyzer and zero length ground clip was used. The direct connection to the ground terminal of the probe was required to eliminate ground lead inductance, thus minimizing measurement error. For measured data related to trace terminations, the ground terminal of the probe had a ground clip wire attached. This was provided for ease of measurement. Since all measured data plots were taken under identical conditions, ground lead inductance is constant and thus, does not affect overall comparison of measured results for this paper. Over 120 measurements were taken. Due to similar configurations for trace lengths and termination methods, only the highest speed device, a Cypress CY7B991 programmable skew clock buffer is used. A schematic representation of the test fixture is shown in Figure 1.



Note: For end termination, the pull-up resistor was removed for parallel and AC. The capacitor was replaced with 0 ohm resistor for Thevenin and parallel.

Figure 1 PCB schematic

It should be noted that the use of the jumpers described above for PCB configuration changes could be responsible for small impedance discontinuities in the test signal path, thereby exacerbating reflections over those reflections that would have been experienced under the ideal conditions of no path discontinuities.

Using the circuit of Figure 1, baseline data was taken to observe the effects of "no" termination; direct trace from driver to load. Results are shown in Figure 2 for both the 3 inch and 18 trace. Measurements for 8" and 13" traces revealed similar results which are not presented in this paper. For purpose of identification internal to the plots, TP1 refers to the output of the driver before the series resistor, TP2, output of the series resistor (if provided), and TP3 at the load. As seen in Figure 2, excessive ringing exists for the 18" trace (scale reference - 2 V/division), while minimal overshoot / undershoot exist for the 3" trace (scale reference - 2V/division). The 18" trace had an overshoot of 7V, and an undershoot of 2V (5V source). This additional voltage amplitude was caused by additive effects of ringing due to reflections in the excessively long trace. This overshoot and undershoot is cause for multiple system problems, which include signal quality and EMI emissions.

Due to difficulties of calculating exact impedance (Z_0) of the trace (design of the board), approximate values of termination resistors were provided. An occasional glitch is observed on various plots because of this minor impedance mismatch.

TERMINATION METHODOLOGIES

Four commonly used termination methods are investigated. These were series, parallel, Thevenin and AC. No one standard termination works best due to complexities of layout, power consumption, component count and unexpected parameters that exist in a PCB. Sometimes, multiple termination methods are provided by design engineers to allow for experimentation on the real PCB.

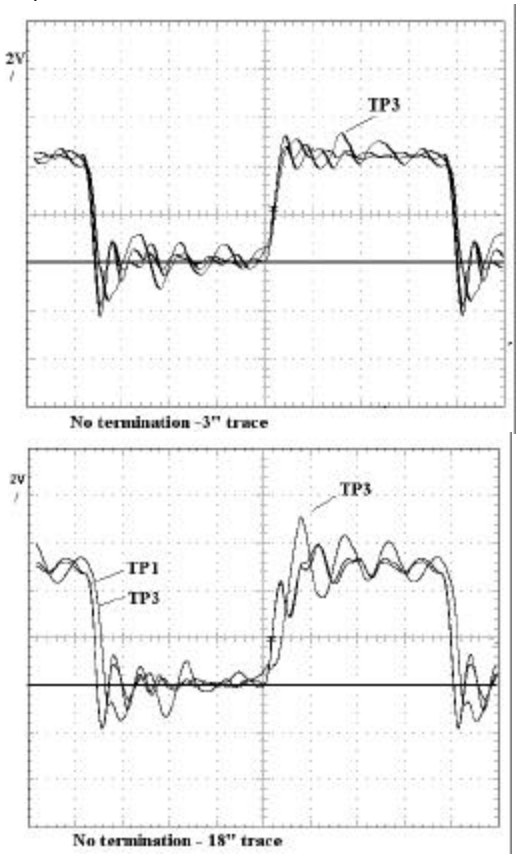


Figure 2 Baseline measurements - no termination

When multiple terminations are used in a design, a series resistor is generally provided along with parallel, Thevenin or AC. We investigate how well each terminations method works by itself, before we add the series resistor to determine effects of multiple terminations.

Series termination

Series termination (also called source termination) is commonly used when a lumped load is at the end of the trace. This termination is best for point-to-point

applications. The device output impedance and series resistor was set to 150 ohms, the approximate loaded characteristic impedance of the trace; double sided board - 0.062" thick. The resistor was located directly at the output of the driver. When a series resistor is used, the impedance of the trace is changed as a function of frequency described by Equation 1 where ω is frequency (in radians), L is series inductance, and C capacitance of the trace. It is observed that when R exceeds ωL, characteristic impedance becomes inversely proportional to the square root of the frequency available. At high frequencies, if ωL exceeds R, characteristic impedance becomes constant.

$$Zo(w) = \left(\frac{R + jwL}{jwC} \right)^{1/2} \qquad (1)$$

The effect of the transmitted voltage level for series termination is detailed in Equation 2. In the plots, this is identified as TP2. Propagation delay at the load (TP3) is described by $t_{pd} = 0.7 (Z_o C_d)$.

$$\Delta Vb = \Delta Va \left(\frac{Zo}{Rs + Ro + Zo} \right) \qquad (2)$$

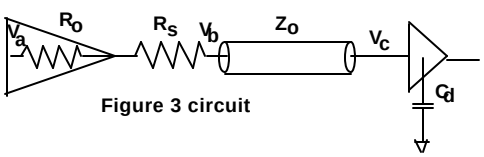


Figure 3 circuit

We compare the 3" trace with the 18" trace, both at 1V/division. With a series resistor, there is minimal ringing at the load (TP3); acceptable waveform available for signal functionality compared to the plots of Figure 2. The increased propagation delay is easily observed compared with the longer trace. The series resistor, (input - TP1, output - TP2) illustrates the masking of these reflections. The reason why both plots look nearly identical is because the circuit behaves identically when properly terminated, regardless of trace length.

Since $R_S + R_O = Z_O$, the voltage level at V_b (TP2) is 1/2 the voltage of V_a.(TP1). The voltage waveform measured is divided evenly with half of the voltage transmitted to the receiver. If the receiver has a very high input impedance, the full waveform will be observed at the load at t_{pd} while the source will receive the reflected waveform at $2 * t_{pd}$ where t_{pd} is the one way propagation delay.

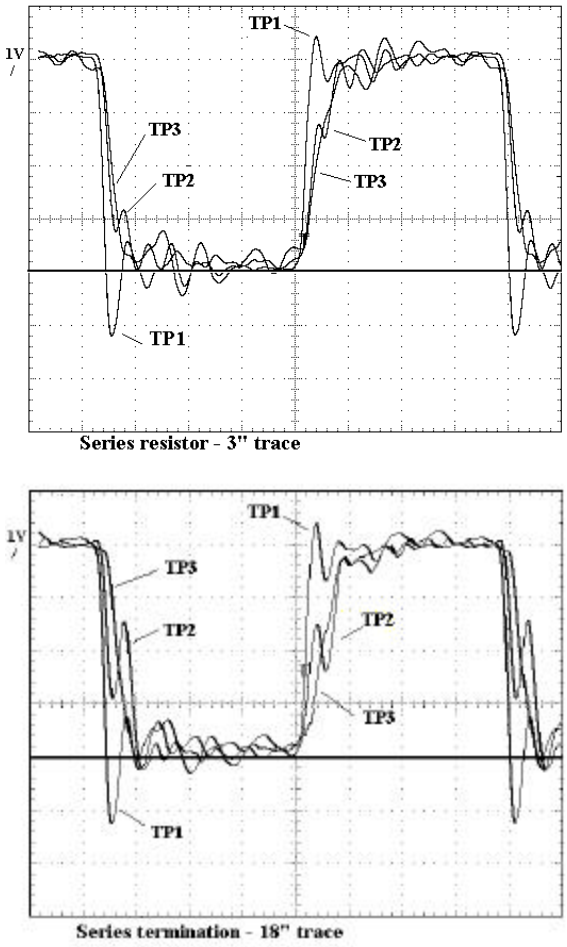


Figure 3 - Measured results of series termination

The 1/2 V_{max} plateau places the signal in an indeterminate logic state which is cause for improper operation should a bus structure be provided with multiple loads at various routed spacings. Signal integrity issues exist for all devices on the bus except for the receiver at the end of the bus.

Parallel termination

For parallel termination, a single pull-down resistor is provided at the load. This allows for fastest circuit performance when driving distributed loads. This resistor has a Z_O value equal to the trace impedance, 150 ohms. The other end of the resistor was tied to ground. A nearly undistorted waveform is observed along the full length of the line at TP3. Overshoot of 1V does exist. Loading a long line should not affect propagation delay of the source driver.

$$\Delta Va = \Delta Vb\left(\frac{Zo}{Ro+Zo}\right) \quad (3)$$

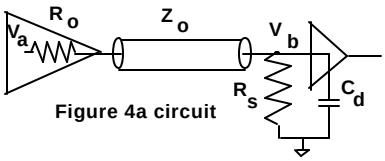
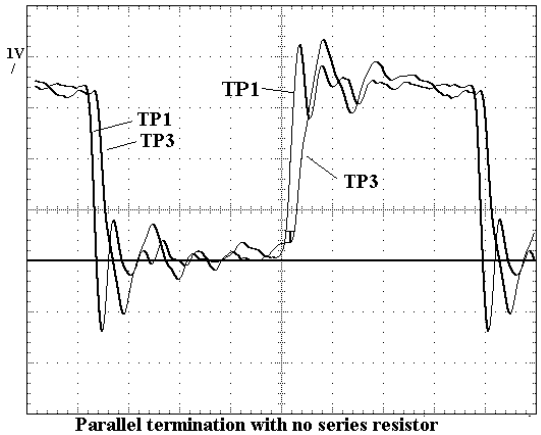


Figure 4a circuit

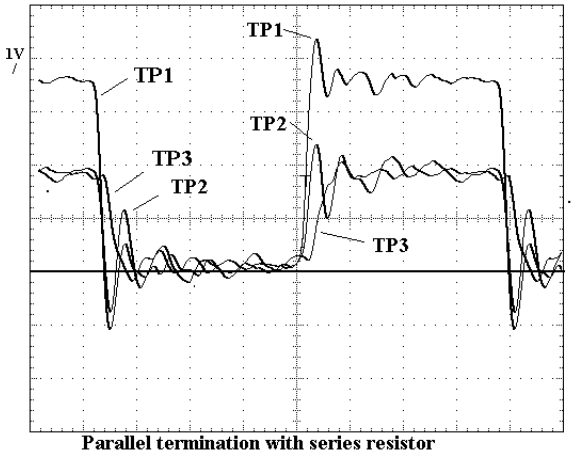


Parallel termination with no series resistor

Figure 4a - Measured results of parallel termination

An increase in delay will be observed on busses with multiple receivers and drivers on the net due to additional lumped capacitance provided by all devices.

With this configuration, a 150 ohm series resistor was added to the network (dual termination). Figure 4b illustrates an unusual effect. The received waveform is at a voltage level of $1/2V_{max}$ which is less than that desired for proper signal functionality in the HI state. The series resistor created this 1/2 voltage level, described by Equation 3. The series resistor did not provide additional masking effects for removal of ringing, overshoot or undershoot if the purpose of adding the resistor was to clean-up the propagated



Parallel termination with series resistor

Figure 4b - Parallel termination with series resistor

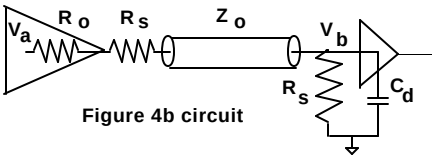


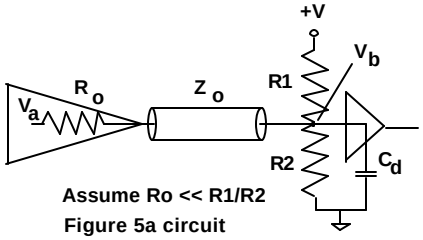
Figure 4b circuit

signal. If a high current driver is provided, the series resistor would allow less voltage and current to exist in the trace. Extrapolating this analysis to the frequency domain, with less RF current, less RF emissions will exist. However, most logic families cannot use this termination because of reduced voltage swing.

Thevenin network

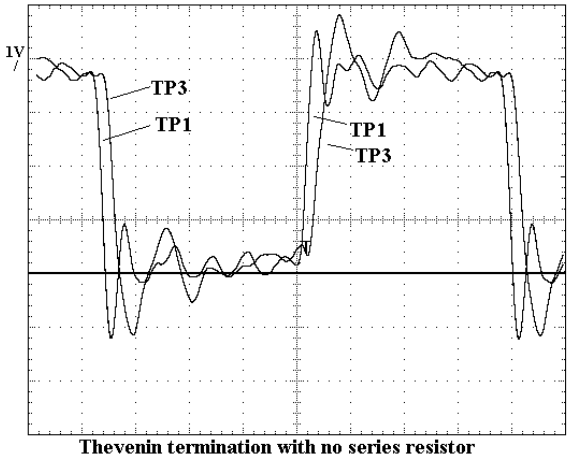
For the Thevenin network, one resistor was connected to power and the other resistor to ground providing a characteristic impedance match of 150 ohms. This termination is rarely used in practice because of the large drive current required in the HI-state. The results in Figure 5a shows a nearly perfect waveform, along with the expected delay of the signal at the load.

$$\Delta Vb = \Delta Va\left(\frac{R2}{R1+R2}\right) \quad (4)$$



Assume Ro << R1/R2

Figure 5a circuit



Thevenin termination with no series resistor

Figure 5a Measured results of Thevenin termination

With this configuration, a 150 ohm series resistor was added to the network (dual termination). Figure 5b illustrates this effect. The voltage waveform was nominal in the HI-state, but in the LO-state, we

observe a voltage level of 1/2 V_{max} due to the effects of the series resistor, discussed earlier. Ringing is minimized at the load (TP3), whereas the output of the series resistor (TP2) bounces around in the transition region on the falling edge.

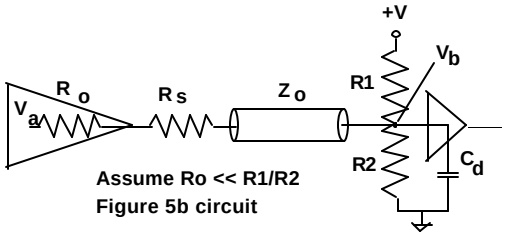
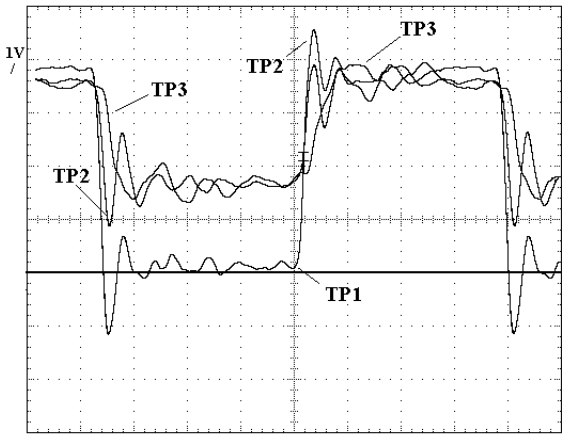


Figure 5b circuit



Thevenin termination with series resistor

Figure 5b Thevenin termination with series resistor

AC Network

This termination method works well in both TTL and CMOS systems. The resistor matches the impedance of the trace. The capacitor holds the DC voltage level of the component. As a result, AC current flows to ground during the switching state. Less power dissipation exist from parallel termination. The resistor must equal the Z_O of the trace. The capacitor is generally very small (20-200 pf). The RC time constant must be greater than twice the loaded propagation delay. RC termination finds excellent use in buses containing similar layouts. The resonance seen in Figure 6a is due to self-resonance of the network with lumped distributed capacitance, inductance of the trace, and component inductance.

$$t = R_S C_S \text{ where } t > 2 * t'_{pd} \quad \text{for optimal performance} \qquad (7)$$

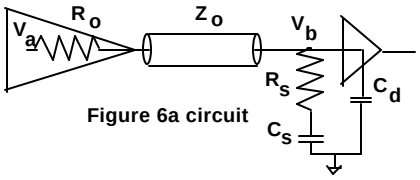
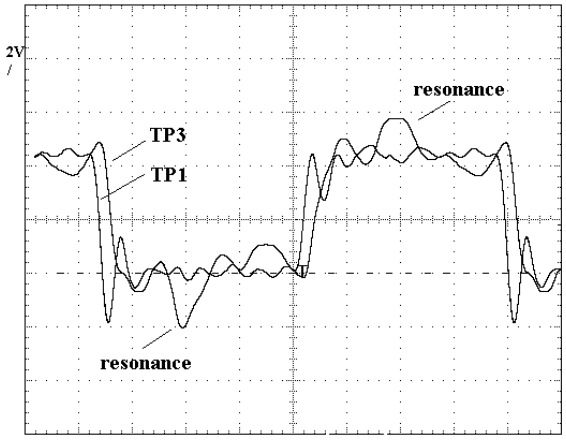


Figure 6a circuit

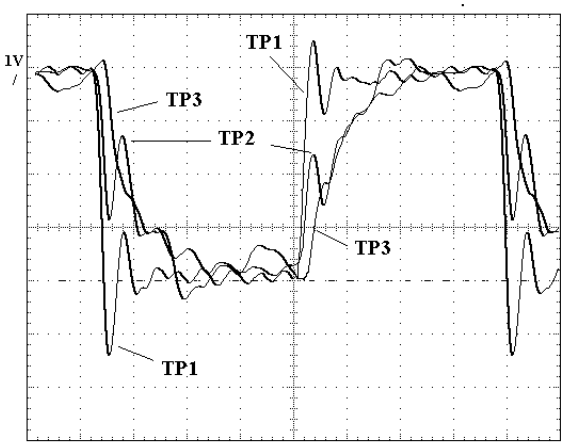
If the round trip propagation delay is 4 nsec, RC must be > 8 ns. Calculate C using known round trip propagation delay and the characteristic impedance of the trace.



AC termination with no series resistor

Figure 6a Measured results of AC termination

A series resistor is now added to the AC terminated trace. Two items are of interest seen in Figure 6b. We still have the effects of the series resistor at 1/2 V_{max}, in addition to a rounded clock signal. Ringing, overshoot and undershoot at the load is, however, minimized.



AC termination with series resistor

Figure 6b AC termination with series resistor

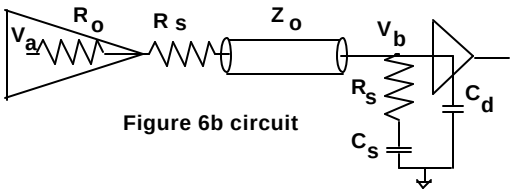


Figure 6b circuit

SUMMARY

Different termination methods are available, each for a specific application along with advantages and disadvantages. The termination method that provides optimal performance for most designs (CMOS or TTL) is dependent on what the circuit designer wants.

1. Series is excellent for point-to-point and short propagation time with respect to clock frequencies (t_{pd}) and for CMOS (low power consuming components). Series termination may also be used to slow down edge times so that the effects of propagation discontinuities in the signal path is minimized.
2. Parallel is preferred for buses and point-to-point nets with fast clock/pulses (frequencies).
3. Thevenin network are difficult to implement due to the reduced voltage level that exist in the HI state if a combination of both CMOS and TTL exist on the same net.
4. AC termination provides good signal quality but at the expense of added components. Drawbacks exist at high frequencies and for long trace lengths due to limited damping that occurs with poor impedance matching.
5. Dual terminations generally degrade signal functionality desired, and should not be used without fully understanding the consequences.

If computer simulation is used to repeat the data presented, differences will exist due to use of real components and actual layout versus theoretical and perfect models generally provided by simulation programs. The data recorded is what would be seen by a design engineer using typical laboratory equipment.

Knowledge of how a PCB functions in the time domain is important for today's products. Optimal design implementation techniques are also required for proper functionality, especially with new, higher speed designs and logic circuits. The items presented in this paper are fundamental concepts. An understanding of termination methods, trace lengths, and their effects on a PCB will help make the design engineer more successful in their professional career.

ACKNOWLEDGMENT

Thanks to HADCO Corporation for providing the printed circuit board used in this research project. Additional acknowledgment to Robin Simpson, PCB designer who designed the board layout, Bill Baldwin for assistance in data acquisition, W. Michael King for technical review, and Whittaker Communications for use of their facilities and support to conduct this research.

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