Signal Integrity & EMC Considerations In Printed Circuit Board Design

(One and Two Day Seminar Versions)

Introduction

This course presents hands-on techniques for the design and layout of printed circuit boards. Signal Integrity and electromagnetic compatibility (EMC) along with regulatory compliance requirements are examined. Signal integrity is a primary concern for system functionality, while EMC compliance allows a product to be legally sold. This course was developed for both experienced and junior level engineers who are responsible for printed circuit board designs and system level products.

The participant upon completion should be able to create a high-density, high technology printed circuit board that meets or exceeds test and system level requirements without rework. Design and layout techniques of several years ago are now insufficient to address today's high speed, high technology products for both signal integrity and EMC.

In an informal atmosphere, design and layout techniques are introduced in an easy to follow step-by-step presentation that allows plenty of opportunities to address specific questions. Major instructional emphasis is placed on real-life examples that demonstrate optimal layout practices that can be incorporated immediately.

Course Objective

Both simplified EMC theory and "rules-driven, hands-on techniques" for enhancement of signal integrity along with suppression of RF energy (EMI) created within the printed circuit board is presented. The focus is at the *fundamental* level. Rigorous mathematical analysis and theory will *not* be presented. The course is geared toward multi-layer, high-density designs. Requirements for single- and double-sided designs are examined based upon fundamental concepts for multi-layer boards. Where applicable, simulations are performed to highlight design requirements for optimal performance.

The course allows engineers to understand how a PCB functions using transmission line theory, how RF energy is created, creating an optimal power distribution network, and to provide insight into concepts and tools during the layout and prototype period. Proper layout not only assures functionality, but also allows for compliance with EMC requirements plus compatibility between electrical systems for both commercial and military applications.

The discussion on EMC, which is a major part of this course, is based on implementing RF suppression at the circuit level instead of relying on system level containment or shielding to prevent undesired electromagnetic interference.

Who Should Attend

This course is intended for *practicing* design engineers of all disciplines, regulatory compliance engineers, EMC consultants and PCB designers. No formal training in electronic theory is required. Concepts, theory and layout techniques are presented in an easy to understand format, *without math*, using practical and real world examples. Engineers, technicians, supervisors and managers can also gain valuable insights into PCB design and layout for today's high technology products along with obstacles that exist for the designer.

Benefits of Attending

- Increased Job Knowledge
- Enhanced Signal Integrity
- Teaches EMC Suppression versus Containment
- Allows First-Time Compliance to EMC Requirements
- Reduce Design Time and Manufacturing Costs
- State-of-the-Art Design and Layout Techniques Presented

About the Instructor

Mark Montrose is principle consultant of Montrose Compliance Services, Inc., a full service regulatory compliance firm specializing in Electromagnetic Compatibility with 30 years of applied EMC experience. Prior to becoming a consultant, Mark was responsible for regulatory compliance for several high-technology companies in Silicon Valley, California. His work experience includes design, test and certification of both Information Technology (ITE) as well as Industrial, Scientific and Medical products (ISM). He is assessed by a European Competent Body to perform CE compliance approval and in situ testing and certification of industrial products.

Mark is a Senior Member of the IEEE and a past member of the *Board of Directors* of the IEEE as Division VI Director (2009-2010). He is also a long-term past Board member of the IEEE EMC Society plus Champion and First President of the IEEE Product Safety Engineering Society. He was a popular distinguished lecturer for the IEEE EMC Society and is considered an expert in printed circuit board design and system level applications for EMC compliance. He has presented numerous papers based on sophisticated research related to printed circuit boards and the field of EMC at International EMC Symposiums and Colloquiums worldwide. Mark also provides personalized in-house seminars and consulting services to corporate clients worldwide in addition to the University of California, Santa Cruz extension program.

Mark has authored the following best-selling text/reference books published by Wiley/IEEE Press.

- *Printed Circuit Board Design Techniques for EMC Compliance*, 1996-1st ed / 2000-2nd ed.
- *EMC and the Printed Circuit Board - Design, Theory and Layout Made Simple*, 1999.
- *Testing for EMC Compliance – Approaches and Techniques*. 2004.
- Contributing author to the *Electronics Packaging Handbook*, Chapter 6, 2000 (CRC/IEEE Press).

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Signal Integrity & EMC Considerations in PCB Design

(One Day Version)

Fundamentals of Signal Integrity
- Lossy and Lossless Transmission Lines
- Relative Permittivity (Dielectric Constant)
- Propagation Delay and Dielectric Constant of Various Materials
- Dielectric Constant Chart for FR-4 Material
- Typical Transmission Line System
- Reflections – Poor Signal Integrity
- Signal Distortion Characteristics
- Crosstalk
- Sample List of Design Techniques to Prevent Crosstalk
- Power and/or Return Bounce
- Typical Bounce Waveform

- **Fundamentals of EMC**
- Basic Aspects and Elements of EMC
- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Closed Loop Circuit
- Radiated Emissions from a Closed Loop Circuit
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- The Need for Flux Cancellation
- Cause of EMC – System and PCB Level
- Summary of EMI Development Within the PCB

Printed Circuit Board Basics
- Microstrip and Stripline Topologies
- Field Distribution for Microstrip and Stripline
- RF Current Density Distribution
- Image Planes
- Ground Slots Created with Through-Hole Components
- Primary Grounding Methodologies
- Ground Loop Control
- Component Selection Related to EMC

Bypassing and Decoupling
- Defining Capacitor Usage
- Capacitors and Resonance
- Using Capacitors in Parallel
- Effects of Capacitors in Parallel-Same Value
- Power and Return Plane Capacitance
- Calcuating Power and Return Plane Capacitance
- Multi-pole Decoupling Methodology
- Radius of Operation
- The Capacitor Bridgade
- Capacitive Loops Created by Decoupling Capacitors

Layer Stackup Assignments
- Single and Double-Sided Recommended Layout
- Multi-Layer Stackup Assignments
- Film and Manufacturing Concerns

Impedance Control and Trace Routing
- Component Placement
- Impedance Control – Microstrip and Stripline
- Calculating Maximum Trace Length for Critical Nets
- Trace Separation and *the 3-W Rule*
- Routing Layers
- Layer Jumping
- Guard and Shunt Traces

Terminations (Signal Integrity Concerns)
- Fundamental Concepts of Trace Termination
- Transmission Line Effects
- Termination Methodologies
- Where to Locate Terminators
- What Happens When One Cannot Terminate

Crossing the Barrier
- Isolation (Moating), Bridging and Violations
- Digital and Analog Partitioning
- Fundamental Reasons that Cause EMI in the PCB

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Printed Circuit Board Design for Signal Integrity and EMC Compliance
(Two Day Version)

Fundamentals of Signal Integrity
- What is Signal Integrity
- Signal Integrity Concerns
- Lossless and Lossy Transmission Lines
- Relative Permittivity (Dielectric Constant)
- Propagation Delay Within Various Materials
- Reflections – Poor Signal Integrity
- Typical Transmission Line System
- Reflections and Signal Distortion Characteristics
- Crosstalk
- Design Techniques to Prevent Crosstalk
- Power and/or Return Bounce and Waveforms

Fundamentals of EMC
- Definition of EMC Terms
- The Decibel, Variations and Pitfalls
- Basic Aspects of EMC
- The EMC Environment
- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Electric and Magnetic Field Impedance
- Closed Loop Circuits
- Radiated Emissions from a Closed Loop Circuit
- Return Current Path of Travel-Multilayer Assembly
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- The Need for Flux Cancellation

Basic EMC Suppression and Grounding Concepts
- Different Grounding Methodologies
- Three Primary Grounding Methodologies
- Resonance in a Multi-Point Ground
- Aspect Ratio-Minimizing Ground Loops
- Image Planes
- RF Current Return and Flux Cancellation
- RF Current Density Distribution
- Ground Slots and Through-Hole Components
- Functional Partitioning
- Components Selection Related to EMC

Layer Stackup Assignments
- Single, Double and Multilayer Assignments
- Film and Manufacturing Concerns

Bypassing and Decoupling (Power Distribution)
- Power Distribution Network Overview
- Capacitor Details; Types, Dielectrics, Functional Use
- Capacitors Characteristic and Self-Resonance
- Effects of Capacitors in Parallel
- Power and Ground Plane Capacitance
- Multi-pole Decoupling Concept
- Decoupling Radius of Operation
- The Capacitor Brigade
- Dipole Effects from Use of Decoupling Capacitors
- Placement Recommendations
- Mounting Pad and Loop Inductance
- Buried Capacitance
- Equivalent Circuit of a PCB

Clocks, Impedance Control and Trace Routing
- Signal Spectra (Fourier Analysis)
- Microstrip and Stripline Topologies
- Impedance Control Equations
- Capacitive Loading
- Calculating Maximum Trace Length for Critical Nets
- Trace Separation and the 3-W Rule
- Trace Routing for Clocks and Signals Using Termination
- Layer Jumping
- Routing Over Split Planes
- Guard and Shunt Traces

Terminations (Signal Integrity Concerns)
- Fundamental Concepts of Trace Termination
- Transmission Line Effects
- Common Termination Methodologies
- Correct Method to Implement Termination

Interconnects and I/O
- Partitioning, Isolation (Moating) and Bridging
- Image Plane or Moat Violation
- Digital and Analog Partitioning, Layout and Filtering
- Filtering and Grounding
- Common-Mode and Differential-Mode Currents
- Multi-Point Grounding (I/O Connectors)
- Video and Audio Circuits

Electrostatic Discharge (ESD) Protection

Backplanes and Daughter Cards
- Design Basics - Five Areas of Concern
- Mechanicals and Interconnects
- Signal Routing and Terminations
- Ground Slots in Backplanes

Miscellaneous Design Techniques/Concepts
- Localized Planes
- Trace Routing for Corners
- The *20-H Rule*
- How to Select a Ferrite Device
- Grounded Heatsinks
- BNC Connectors
- Lithium Battery Circuits
- Creepage and Clearance Distances