Power and Ground Bounce Effects on Component Performance Based on Printed Circuit Board Edge Termination Methodologies

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Abstract

Printed circuit boards (PCBs) are one source of radiated EMI with digital components the culprits. To minimize development of common-mode currents within the silicon package of large current consuming circuits, a stable power distribution network (PDN) is required. Any noise (bounce) on either the power or 0V reference (ground) plane may cause simultaneously switching noise (SSN) or signal integrity (SI) problems, as well as EMI. In addition, if planar bounce exceeds margin levels, components may not function. To ensure a stable PDN is present, decoupling capacitors and buried capacitive structures are mandatory, along with minimizing loop inductance.

The uniqueness of this research lies in analyzing planar bounce that may exceed voltage margin levels from reflected EM waves that propagate *back* to components from the physical edge of the PCB. The edges of a PCB are in reality a high-impedance, non-terminated signal transmission line stub. With each reflection, ringing occurs. The magnitude of this ringing may cause digital components to have SSN and/or EMI problems.

Popular board edge termination techniques are invested to determine if a designer should be concerned with reflected wave switching noise on either a power or 0V reference plane, which *cannot* be removed by capacitive structures or decoupling.

Index Terms— Printed circuit board (PCB), board edge radiated emissions, 20-H Rule, RC plane termination, power bounce, ground bounce, SSN, SI.

INTRODUCTION

The primary source of common-mode radiated EMI emanates from the silicon die of digital components. The majority of operational problems (SI and EMI) are due to having a poor power/return distribution network (PDN). With a poor PDN, simultaneous switching noise is present, created when voltage levels exceeds operational parameters. Switching noise on planes is generally referred to as bounce, when analyzed in the time domain.

Power and return planes function as transmission lines, and operate no different than signal traces [1, 2]. These planes must be terminated in their characteristic impedance or a reflected wave will bounce back to its source after hitting a high-impedance load, which happens to be the physical edge of the assembly. Depending on phasing of multiple outgoing and reflected waves, phase addition or subtraction may occur along with ringing. If the additive value of the ringing exceeds threshold levels of a component's power/return pins, functional problems may occur. This paper investigates this unique aspect of power distribution corruption to digital components.

There are two causes of planar bounce, one from poor decoupling and the other from reflective wave switching which "cannot" be removed by capacitive structures, but by properly terminating a transmission line (planes) at the physical edge of the PCB.

Details on board edge radiated emissions when analyzed as a transmission line is presented in [2]. This paper examined the radiated effect of a propagating field *away* from the PCB edge. This research uses the identical configuration except with different observation points to examine what happens when an EM field does not radiated *from* the edge of the PCB but is reflected *back* to the center of the assembly.

There are three primary means of terminating planes; via stitching [3], use of discrete RC components (nearly impossible to implement but simulated herein), or the 20-H Rule (x-H) [1, 2]. The x-H Rule is a simple but complex design technique that if implemented correctly minimizes near-field board edge radiated coupling to adjacent assemblies. We use both the x-H Rule and RC terminations to determine if a reflected wave from the edge of the board will cause excessive voltage fluctuations on the power plane, which in turn may cause SSN and EMI. Decoupling will not remove reflective wave problems due to un-terminated transmission line behavior; a completely different problem.

A real PCB has numerous stimulus sources. Attempting to analyze a PCB with only one source stimulus provides *limited* or *minimal* value to designers. For this research, we use multiple stimuli simultaneously at different frequencies to emulate a real PCB, and not a simplified model. To determine if the reflected wave back to both the core and I/O pins of a VLSI component exceeds threshold levels causing both SI and EMI problems, we use HFSS, a Finite Element Method simulation program by Ansoft Corp.

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TEST CONFIGURATION AND MODEL

The test configuration is illustrated in Figures 1 and 2. In Fig. 1, *S1*, *S2* and *S3* are the physical location of three stimulus sources. The small solid rectangles denote five observation points (Obv.) - P(x). Figure 2 illustrates the model used for simulation. Results from [2] detail why a shield plane is required above the power plane; to prevent z-axis EMI. If the x-H Rule is used on a 4-layer PCB, implementation will result in the deliberate design of a patch antenna thus, x-H is valid only for a 10 or more layer PCB, and also only when a shield plane is provided.

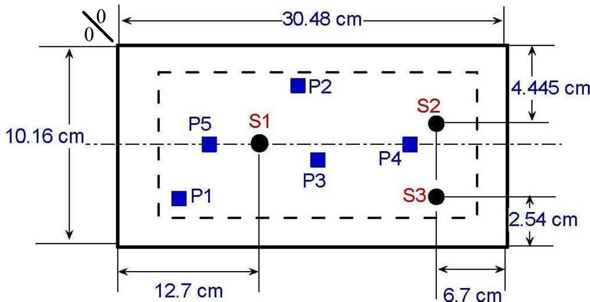

Figure 1. PCB configuration of planes (not to scale).

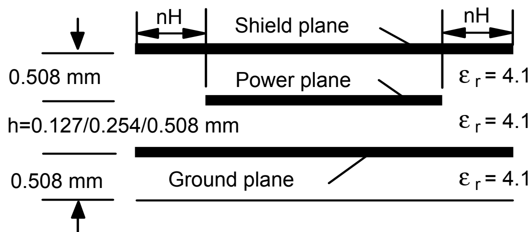

Figure 2. Simulation configuration.

The five observation points [P(x)] represents where a digital component may be physically located that could be subjected to switching noise on the power plane from reflected waves returning from the board edge. These observation points are listed in Table 1.

Table 1. Location of the five observation points.

Port #	X Coordinate (cm)	Y Coordinate (cm)
P1	8.5	2.0
P2	2.5	14.0
P3	6.0	15.24
P4	5.08	20.0
P5	5.08	6.7

In Figure 3, we observe both an external propagating board edge radiated emission [2] as well as a reflected wave back into the middle of the board.

In a real PCB there are always more than one digital component switching logic states at the same time. Depending upon the physical distance between a component and the edge of the assembly, additive phasing of multiple reflected waves may be observed somewhere in the middle of the PCB. If a large amount of noise voltage exist at the power or return (ground) pins beyond operational margins, system failure may occur.

<u>The test parameters for simulation are</u>:

Distance spacing between power/return planes (h):
0.127 / 0.254 / 0.508 mm (5/10/20 mils)
Stimulus: 300/600/900 MHz and 1.2/1.5 GHz
Stimulation: 1-amp current source between the planes.
Source and observation point locations: See Figure 1.

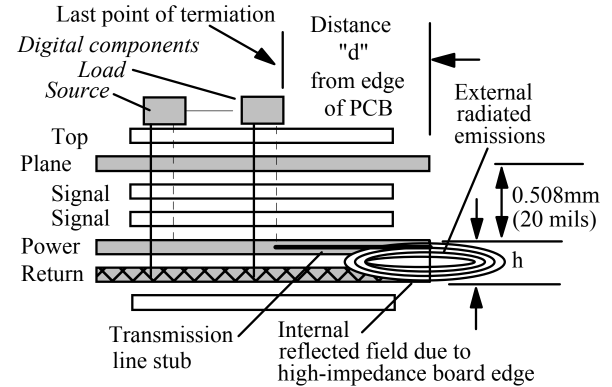

Figure 3. Transmission line visualization of planes.

IMPEDANCE ANALYSIS OF THE PCB

Figure 4 and Table 2 illustrates the impedance (|Z|) of the PCB based on numerical simulation. The further apart the planes are separated, the higher the value [2]. The impedance will also vary significantly depending on the physical dimensions of the PCB.

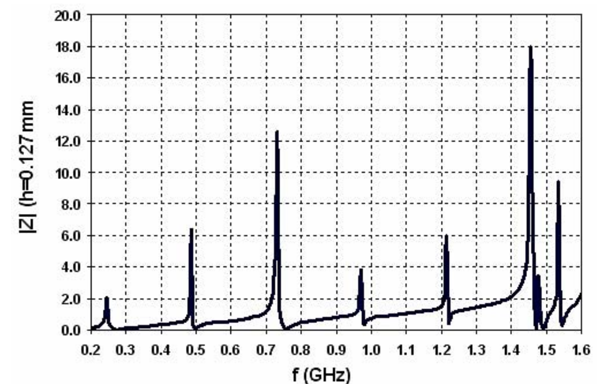

Figure 4. Resonant frequencies of the PCB model.

Table 2. Impedance of the PCB, different configurations.

Frequency	Distance spacing between planes		
	h=0.127 mm	*h=0.254 mm*	*h=0.508 mm*
0.3 GHz	0.13 ohms	0.25 ohms	0.50 ohms
0.6 GHz	0.59 ohms	1.19 ohms	2.38 ohms
0.9 GHz	0.79 ohms	1.59 ohms	3.18 ohms
1.5 GHz	0.61 ohms	1.22 ohms	2.45 ohms

ANALYSIS 1: USING X-H RULE TERMINATION

To determine the magnitude of an RF field reflected back into the center of the PCB, three different x-H spacings between power and return plane with three "simultaneous" stimulus (*S1*-*S3*) were analyzed. By examining a large matrix of data, we can determine total effects of phasing of multiple reflected waves from the board edge at various physical locations where digital components might be placed.

In Tables 3, 4 and 5, each observation point is identified as P(x) with various values of x-H termination. Plots are provided (Figure 5) to help visualize the magnitude of the bounce voltage to simplify understanding what is occuring in the PCB.

Interesting results appear in the Tables and Figure 5. It is obvious that the magnitude of the power plane bounce easily exceeds operational margins of most digital components, *but only if planar resonance is present*, depending on physical dimensions of the PCB.

EMI (common-mode currents) may also be radiated from the component's silicon/package if noise voltage margins exceed operational parameters. For certain physical dimensions, in consonant with distance separation between the power and return planes and their resonance frequencies, potential SSN and EMI is possible. For some configurations, as much as several volts of bounce will be present! All voltage levels above 1 Volt are highlighted in Tables 3-5 in bold face.

Noise voltage (bounce) 1 Volt and above is more prevalent when the distance spacing between the planes is greater that 0.127mm (5 mils).

ANALYSIS 2: USING RC TERMINATION

To compare whether the x-H Rule provides enhanced power bus noise reduction, we substituted an RC network (R=2 ohms, C=20 pF) at the physical edge of the PCB using the 0-H configuration, which is the only implementation method for this termination technique (x-H Rule). The two sides along the y-axis has nine (9) RC pairs. The two sides along the x-axis has four (4) RC pairs for a total of 26 terminations. Simulation was performed at the same frequencies as before with results tabulated in Tables 6, 7 and 8.

We learn that using an RC termination network to minimize planar bounce internal to the PCB is superior to x-H for most configurations. The areas where x-H *does performs better* is highlighted in bold face in Tables 6-8, which was infrequent. At 1.2 GHZ, for almost all configurations, *a significant amount of noise voltage was present due to the board having a high impedance at this frequency*. Simulating a PCB at both resonant and non-resonant frequencies provides valuable data when analyzing cause and effect in a conceptual manner.

Table 3. Maximum bounce voltage with ***h*=0.127 mm**

Obv. Pt.	**300 MHz**	**600 MHz**	**900 MHz**	**1.20 GHz**	**1.50 GHz**
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-10h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P1-20h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P2-0h	0.10 V	0.23 V	0.34 V	**2.59 V**	0.41 V
P2-10h	0.10 V	0.22 V	0.50 V	**2.11 V**	0.43 V
P2-20h	0.10 V	0.22 V	0.35 V	**1.59 V**	0.80 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-10h	0.15 V	0.18 V	0.22 V	0.24 V	**1.60 V**
P3-20h	0.16 V	0.18 V	0.56 V	0.09 V	0.16 V
P4-0h	0.38 V	0.17 V	0.10 V	**1.91 V**	0.47 V
P4-10h	0.17 V	0.01V	0.18 V	**2.30 V**	**7.14 V**
P4-20h	0.41 V	0.19 V	0.12 V	**1.25V**	**2.11 V**
P5-0h	0.16 V	0.01V	0.19 V	**2.72 V**	0.45 V
P5-10h	0.17 V	0.01 V	0.18 V	**2.30 V**	**7.14 V**
P5-20h	0.19 V	0.01 V	0.15 V	**1.76 V**	0.40 V

Table 4. Maximum bounce voltage with ***h*=0.254 mm**

Obv. Pt.	**300 MHz**	**600 MHz**	**900 MHz**	**1.20 GHz**	**1.50 GHz**
P1-0h	0.47 V	0.21 V	0.49 V	**0.97 V**	0.49 V
P1-10h	0.53 V	0.20 V	**1.24 V**	**1.06 V**	0.84 V
P1-20h	0.63 V	0.19 V	0.32 V	0.88 V	**9.45 V**
P2-0h	0.19 V	0.46 V	0.67 V	**4.69 V**	0.81 V
P2-10h	0.20 V	0.45 V	0.81 V	**3.21 V**	**1.43 V**
P2-20h	0.20 V	0.43 V	0.12 V	**2.49 V**	**10.0 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	**1.19 V**
P3-10h	0.31 V	0.36 V	**1.17 V**	0.09 V	0.61 V
P3-20h	0.33 V	0.38 V	0.74 V	0.31 V	**13.7 V**
P4-0h	0.75 V	0.34 V	0.21 V	**3.48 V**	0.75 V
P4-10h	0.81 V	0.37 V	0.23 V	**2.57 V**	**3.94 V**
P4-20h	0.89 V	0.40 V	0.23 V	**2.08 V**	**13.3 V**
P5-0h	0.32 V	0.02 V	0.38 V	**4.96 V**	**1.03 V**
P5-10h	0.37 V	0.01 V	0.32 V	**3.64 V**	**1.04 V**
P5-20h	0.44 V	0.01 V	0.26 V	**2.89 V**	**9.39 V**

Table 5. Maximum bounce voltage with ***h*=0.058 mm**

Obv. Pt.	**300 MHz**	**600 MHz**	**900 MHz**	**1.20 GHz**	**1.50 GHz**
P1-0h	0.97 V	0.42 V	**1.21 V**	**1.68 V**	0.64 V
P1-10h	**1.17 V**	0.39 V	0.21 V	**1.76 V**	**33.8 V**
P1-20h	**1.63 V**	0.36 V	**121.5V**	0.65 V	0.19 V
P2-0h	0.38 V	0.92 V	**1.52 V**	**8.38 V**	**1.97 V**
P2-10h	0.40 V	0.88 V	0.52 V	**5.41 V**	**41.9 V**
P2-20h	0.40 V	0.86 V	**106.8V**	**3.26 V**	**2.08 V**
P3-0h	0.58 V	0.70 V	**1.06 V**	0.38 V	**3.63 V**
P3-10h	0.64 V	0.74 V	**1.38 V**	0.39 V	**61.8 V**
P3-20h	0.73 V	0.78 V	**45.51V**	0.45 V	0.11 V
P4-0h	**1.52 V**	0.69 V	0.44 V	**6.26 V**	**1.29 V**
P4-10h	**1.70 V**	0.76 V	0.47 V	**4.47 V**	**61.5V**
P4-20h	**2.07 V**	0.87 V	**3.74 V**	**3.82 V**	**1.24 V**
P5-0h	0.68 V	0.04 V	0.73 V	**9.02 V**	**1.99 V**
P5-10h	0.82 V	0.02 V	0.56 V	**6.20 V**	**41.5 V**
P5-20h	**1.20 V**	0.01 V	2.09 V	**5.22 V**	0.57 V

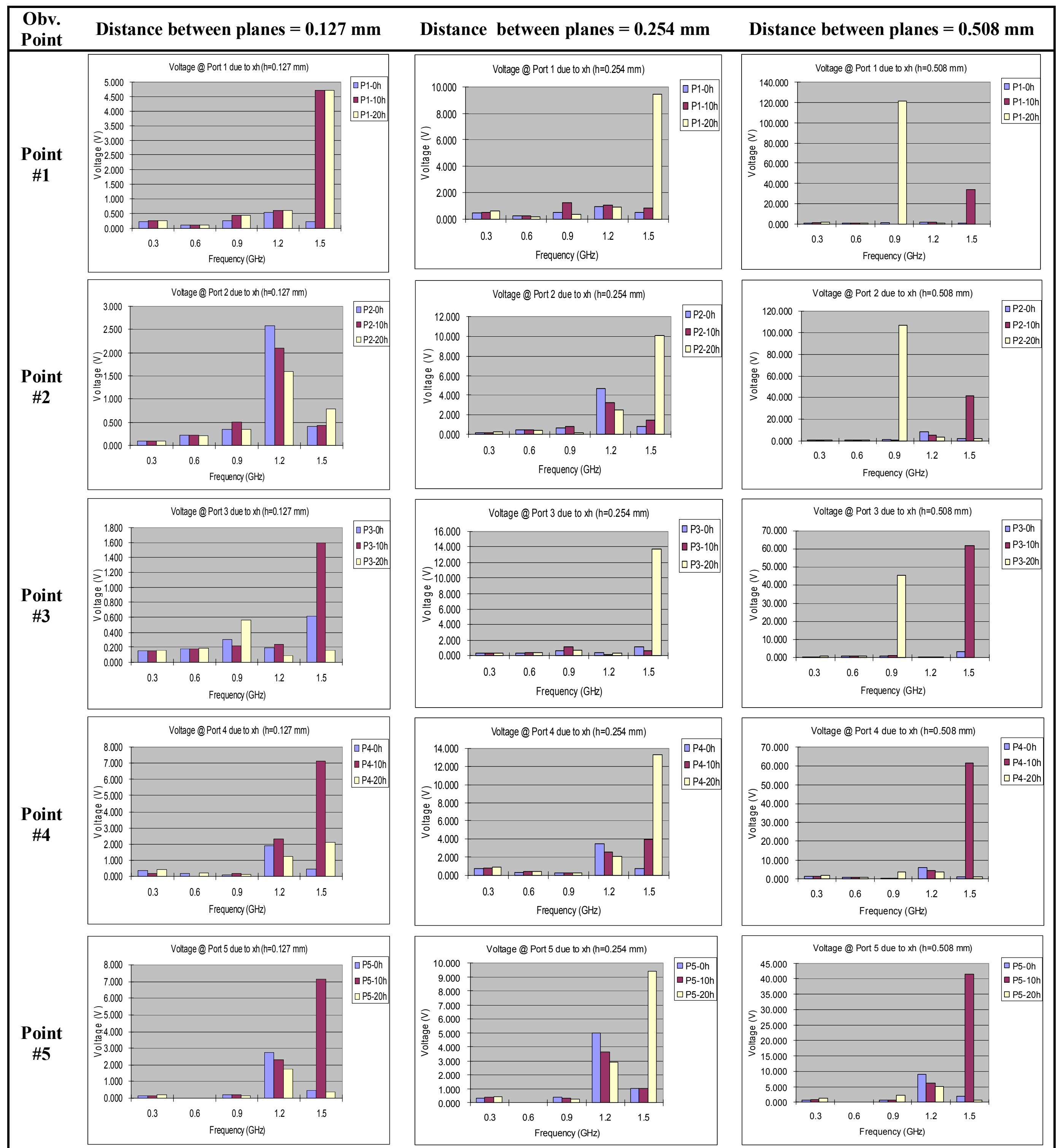

Figure 5. Planar noise using the x-H Rule at all observation points. (Large values indicate possible system failure due to SSN)

ANALYSIS 3: DIFFERENT FREQUENCIES

To analyze further the effects of terminating the physical edge of the PCB to minimize reflected waves back into the center of the PCB, we now simulate with three different frequencies simultaneously to observe phasing effects at our five observation points. Results are presented in Table 9. Only the distance spacing of 0.127 mm is provided for brevity purposes. All voltage levels greater than 0.5V is highlighted in bold face to show the effects of the board's self-resonant frequency related to the creation of planar bounce and its capability to cause circuits to malfunction due to SSN.

Note-Bold face values in Tables 6-8 indicates x-H Rule is superior to RC termination for this configuration.

Table 6. Maximum bounce voltage with ***h*=0.127 mm** and (24) RC termination (R=2 ohms, C=20 pF).

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-0hRC	0.09 V	0.04 V	0.16 V	0.19 V	0.09 V
P2-0h	0.10 V	0.23 V	0.34 V	2.59 V	0.41 V
P2-0hRC	0.08 V	**0.26 V**	0.31 V	0.38 V	0.27 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-0hRC	0.11 V	0.13 V	**0.41 V**	**0.26 V**	0.35 V
P4-0h	0.38 V	0.17 V	0.10 V	1.90 V	0.47 V
P4-0hRC	0.26 V	0.10 V	**0.21 V**	0.09 V	0.36 V
P5-0h	0.16 V	0.01 V	0.19 V	2.72 V	0.45 V
P5-0hRC	0.06 V	**0.04 V**	**0.38 V**	0.34 V	0.11 V

Table 7. Maximum bounce voltage with ***h*=0.254 mm** and (24) RC termination (R=2 ohms, C=20 pF).

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.47 V	0.21 V	0.49 V	0.97 V	0.49 V
P1-0hRC	0.06 V	0.10 V	0.10 V	0.28 V	0.30 V
P2-0h	0.19 V	0.46 V	0.67 V	4.69 V	0.81 V
P2-0hRC	0.12 V	0.27 V	0.10 V	0.44 V	**1.15 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	1.19 V
P3-0hRC	0.15 V	0.32 V	0.05 V	0.07 V	0.92 V
P4-0h	0.75 V	0.34 V	0.21 V	3.48 V	0.75 V
P4-0hRC	0.38 V	**0.35 V**	**0.40 V**	0.81 V	**0.79 V**
P5-0h	0.32 V	0.02 V	0.38 V	4.96 V	1.03 V
P5-0hRC	0.03 V	**0.12 V**	0.22 V	0.70 V	0.51 V

Table 8. Maximum bounce voltage with ***h*=0.508 mm** and (24) RC termination (R=2 ohms, C=20 pF).

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.97 V	0.42 V	1.21 V	1.68 V	0.64 V
P1-0hRC	0.26 V	0.02 V	0.06 V	1.03 V	**2.10 V**
P2-0h	0.38 V	0.92 V	1.52 V	8.38 V	1.97 V
P2-0hRC	0.13 V	0.10 V	0.53 V	0.57 V	**3.66 V**
P3-0h	0.58 V	0.70 V	1.06 V	0.38 V	3.63 V
P3-0hRC	0.15 V	0.23 V	**1.08 V**	**0.96 V**	1.71 V
P4-0h	1.52 V	0.69 V	0.44 V	6.26 V	1.29 V
P4-0hRC	0.37 V	0.47 V	**1.89 V**	0.99 V	**1.96 V**
P5-0h	0.68 V	0.04 V	0.73 V	9.02 V	1.99 V
P5-0hRC	0.09 V	**0.10 V**	0.27 V	1.06 V	**2.58 V**

VALIDATION OF SIMULATED DATA

For all the simulations, a 1A current source was provided at each stimulus port. To validate HFSS, we now use only one current source (1A) at Port *S1* with the observation point at Port *P3*. A rectangular air box enclosing the PCB is used to implement the radiation boundary condition required for the HFSS software.

The solid line in Figure 6 is the simulated results obtained. Analytical results obtained using the formula detailed in [5] are identified by triangles. Validation of the model with numerical simulation is thus confirmed.

Use of the superposition principal is also valid for linearity for components placed anywhere on the PCB.

Table 9. Maximum voltage bounce with three different stimulus sources simultaneously, ***h=0.127 mm***

Obv. Point	S1 (0.3GHz) S2 (0.6GHz) S3 (0.9GHz)	S1 (0.6GHz) S2 (0.9GHz) S3 (1.5GHz)
P1-0h	0.49 V	0.31 V
P1-10h	**0.62 V**	0.39 V
P1-20h	**0.63 V**	0.14 V
P2-0h	0.25 V	0.44 V
P2-10h	0.36 V	0.48 V
P2-20h	0.37 V	0.39 V
P3-0h	0.21 V	**0.50 V**
P3-10h	0.14V	**0.53 V**
P3-20h	0.40 V	**0.82 V**
P4-0h	0.08 V	0.44 V
P4-10h	0.08 V	0.46 V
P4-20h	**0.87 V**	0.62 V
P5-0h	0.34 V	0.27 V
P5-10h	0.34 V	0.26 V
P5-20h	0.33 V	0.42 V

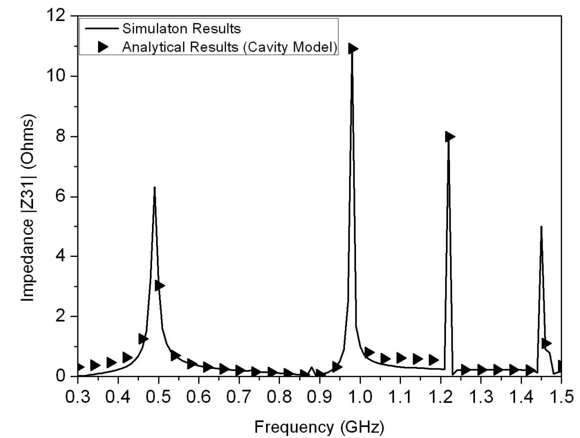

Figure 6. Validation of simulation results and setup.

COMMENTS ON TEST DATA ANOMALY

Several voltage bounce values in Tables 4 and 5 are extremely high to the point of being unrealistic. This is due to the complex impedance present within the planes and what can result when one relies exclusively on simulation to determine if a potential problem may occur. Figure 6 shows the magnitude of the transfer impedance (|*Z31*|) of the PCB model. This Figure validates our previously simulated value of planar impedance (Fig. 4) using a different technique.

To illustrate why large voltage values occur, for example, we excite the plane pair at *S1* using current *I1*, with a voltage response *V3* at *P3* per Eq. (1).

$$Z_{31} = \frac{V_3}{I_1} \text{ (ohms)} \tag{1}$$

From Figure 6, at 0.98 GHz, |*Z31*| impedance is approximately 11 ohms. Exciting *S1* with a 1A current source, the voltage response (magnitude) at *P3* will be 11 volts. This 11 Volt is the amplitude or magnitude of the voltage present because planar impedance is a complex number. We can easily change the y-axis of Table 6 to $V_{magnitude}$ in volts, which is how all data in Tables 3-9 is presented. Any resonance in a PCB can cause large values of planar bounce per Ohm's law.

When phasing multiple stimulus sources at a resonant frequency with a complex impedance, anomalies may occur. The data herein illustrates a *theoretical situation*. This does not mean planar bounce in tens of volts will exist in a real PCB, as numerous losses are present to prevent this from happening. Also, there are generally thousands of reflected waves being reflected back into the middle of the board from many components switching logic states simultaneously. Phasing of many signals at the same time generally result in little SSN.

When using simulation to analyze the "big picture" sometimes results may seem unreasonable but are acceptable if they can be explained. An unexpected value may never be discovered if a massive amount of data is not examined and the mathematics behind the process to achieve these results is solid.

In reality, PCBs utilize decoupling capacitors. Discrete capacitors pull the impedance of a plane pair down to a small value, usually in the order of 1 ohm or less, but *only* within a limited bandwidth of operation. What is discovered in this paper is that with a bare assembly, a SSN problem *may occur if the impedance of the board is high at a particular physical location, which is not lowered by use of discrete decoupling capacitors or a buried capacitive structure*.

CONCLUSION

A real-world PCB has numerous stimulation sources, namely digital components. All components source current from a power plane and sink current to a return plane. Power and return planes behave identical to signal transmission lines and must be treated as such. Un-terminated transmission lines can cause signal integrity problems (SSN) as well as EMI. To ensure system level functionality, every transmission line must be terminated. For plane termination there are several techniques. Two common plane termination techniques were used to analyze planar bounce and if plane pairs need to be terminated to minimize SI and EMI problems; x-H Rule and RC.

What is interesting to see is that no matter what kind of simulation is performed to ascertain if a particular type of board edge termination methodology either enhances or degrades performance, results will vary based on stimulus source location, observation points, distance spacing between planes, physical dimensions of the planes, voltage amplitude of the stimulus source(s), the stub length of each transmission line relative to the physical edge of the board, and numerous other second and third order effects. Basically, a designer must determine all resonant frequencies and phasing effects of reflected waves from the edge of the PCB back to the center before beginning a full board-level simulation, and also how each stimulus source behaves based upon multiple source frequencies. This requires extensive computing resources. To fully understand a problem, dozens of simulations must be performed and analyzed with decoupling capacitors and digital components loading the power distribution network in addition to any transmission line stubs that may exist due to component placement.

Using transmission line theory and applying it to planes, a transmission line stub will exist between the physical location of a component and the board edge, driving this stub as a dipole antenna at switching frequencies. Because of this stub, a reflected wave with a ringing voltage may be observed by digital components located elsewhere within the PCB during a state transition.

When single or multiple stimulus sources are present representing a real-world PCB, an increase in noise voltage ringing on the power/return plane may occur somewhere in the form of planar bounce, which may exceed operational voltage margins regardless of the type of plane termination methodology used, if any, but only if the impedance at a physical location is high due to insufficient decoupling, which lowers plane impedance at that specific point.

With this situation one may encounter possible system failure due to poor signal integrity along with creation and propagation of EMI. Where we physically place our observation point(s) or components is important when considering if plane termination is required to minimize SSN and EMI.

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