Voltage and Return Plane Bounce Affecting Digital Components Using Different Printed Circuit Board Edge Termination Methodologies

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***Abstract*—This paper illustrates effects of board edge termination related to development of either voltage or return plane bounce exceeding operational margin levels of digital components at multiple locations within a printed circuit board (PCB). We study an actual problem encountered by design engineers using a worse-case configuration. This paper also explains how power and/or return bounce is developed. Lack of optimal plane termination at the physical edges of a PCB will exacerbate plane bounce. In addition, a solution that prevents this problem is provided in Section VIII.**

***Index Terms*—Ground bounce, power bounce, power distribution network (PDN), printed circuit board (PCB), signal integrity (SI), simultaneously switching noise (SSN).**

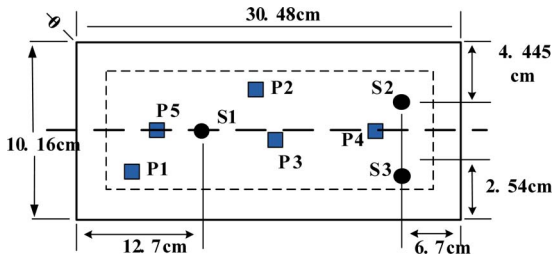

Fig. 1. Location of source and observation points.

I. Introduction

BOTH signal integrity (SI) and electromagnetic interference (EMI) must be considered simultaneously during layout of any printed circuit board (PCB). A poor power distribution network (PDN) is one cause of SI problems along with the development of unwanted EMI. Both voltage and return planes allow a bounce condition to exist if there is insufficient decoupling or a poor PDN for digital components. Plane bounce, or simultaneously switching noise (SSN) if significant, can cause digital components to malfunction.

The physical distance between placement of digital components and the edge of the PCB creates an unterminated transmission line stub. This stub functions as the driven element of a dipole antenna. We investigate both time- and frequency-domain harm caused due to this unterminated transmission line stub that exist on both the power and return planes.

The physical end of a transmission line, if not terminated, presents a high-impedance load to a source driver [1]. Reflections may occur along with possible ringing, depending on transmission line characteristics if the transmission line is electrically long. Every time a digital component sources or sinks current during an edge transition, propagating electromagnetic fields are generated on the power and return planes.

Depending on the phasing of multiple outgoing and reflected waves created from each power and return pin of all digital components, wave addition or subtraction will occur. If the amplitude of phase addition (bounce) exceeds component voltage margin tolerance levels, the system may exhibit functional perturbations seemingly at random. Voltage and return planes thus require termination, the same as electrically long signal traces.

This paper investigates this unique aspect of power distribution corruption to digital components due to lack of, or improper implementation of decoupling capacitors that lowers plane impedance.

Two different termination methodologies were located at the physical edge of the PCB for both the voltage and return planes. HFSS simulation determines the magnitude of plane bounce from both terminated and nonterminated configurations. When evaluating plane bounces, there are two primary areas of concern:

1) external board edge radiated emission coupling to adjacent metallic structures in the near field (not investigated herein) [2];
2) reflected waves on the power and return planes that occur from the edge of the PCB *back into the center of the PCB* producing plane bounce (the focus of this paper).

Three primary means of terminating planes exist: via stitching [3], use of discrete *RC* components [5], [6] (nearly impossible to implement but simulated herein), or different configurations of the x-H rule (x-H) [2], [4].

II. Test Configuration and Model

We analyze a PCB using three simultaneous stimuli all in phase. Fig. 1 details the PCB model, where *S*1, *S*2, and *S*3 are the physical location of three stimulus sources. The solid rectangles denote five observation points (Obv.) – $P(x)$. For the *RC* termination methodology, the power plane is not recessed ($0H$), where "H" is actual distance separation between power and return planes.

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TABLE I
PHYSICAL LOCATION: FIVE OBSERVATION POINTS

Port #	X Coordinate (cm)	Y Coordinate (cm)
P1	8.5	2.0
P2	2.5	14.0
P3	6.0	15.24
P4	5.08	20.0
P5	5.08	6.7

The observation points [$P(x)$] (see Table I) represent possible physical locations of digital components. These devices will encounter plane bounce from propagating waves returning from the physical board edge, reflected back into the center of the PCB, if some form of plane edge termination is not provided.

Simulation parameters

1) *Distance spacing between voltage/return planes (h):* 0.127 / 0.254 / 0.508 mm (5/10/20 mils).
2) *Stimulus:* 300/600/900 MHz and 1.2/1.5 GHz.
3) *Stimulation:* 1-A current source between the planes.
4) *Source and observation point locations:* see Fig. 1.
5) *Relative phase of the three stimulus sources:* In phase.
6) *Domains:* Time for bounce; frequency for wave effect.

III. RESULT #1: X-H RULE TERMINATION

Tables II–IV list each observation point [$P(x)$] with various x-H configurations, any of which could be the physical location where digital components might be located.

For some configurations, several volts of bounce exist. Voltage levels above 1 V are highlighted, which become more prevalent when the distance spacing between the voltage and return planes is greater than 0.127 mm (5 mils). There are no decoupling capacitors provided during this worse-case analysis to simulate a poor PDN design.

IV. RESULT #2: *RC* TERMINATION

An *RC* termination network is now examined to determine which method provides enhanced power bus noise reduction for board edge reflected waves. A series *RC* network ($R = 2\ \Omega$ and $C = 20$ pF) is placed at the physical edge of the PCB. Two sides along the *y*-axis have nine *RC* pairs and the *x*-axis has four *RC* pairs—total of 26 terminations. Simulation was performed at the same frequencies with results tabulated in Tables V–VII. This *RC* value is chosen to match the board impedance, as described in [5] and [6].

The *RC* termination network is notably superior for minimizing planar bounce than most variations of the x-H rule.

To implement *RC* termination, use simulation software or actual measurement to determine plane impedance, which is typically only a few ohms in value. Incorporate this impedance value as a resistor in series with a capacitor, calculated in the same manner as if terminating a single-ended transmission line. The *RC* termination method requires numerous discrete components around the edge of the PCB and is *not* a cost effective means of providing plane termination, nor easily manufacturable.

Tables II–IV: x-H rule, where "0h" represents no termination. (Shaded represents values > 1 V).

TABLE II
MAXIMUM VOLTAGE BOUNCE, $h = 0.127$ mm

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-10h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P1-20h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P2-0h	0.10 V	0.23 V	0.34 V	**2.59 V**	0.41 V
P2-10h	0.10 V	0.22 V	0.50 V	**2.11 V**	0.43 V
P2-20h	0.10 V	0.22 V	0.35 V	**1.59 V**	0.80 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-10h	0.15 V	0.18 V	0.22 V	0.24 V	**1.60 V**
P3-20h	0.16 V	0.18 V	0.56 V	0.09 V	0.16 V
P4-0h	0.38 V	0.17 V	0.10 V	**1.91 V**	0.47 V
P4-10h	0.17 V	0.01V	0.18 V	**2.30 V**	**7.14 V**
P4-20h	0.41 V	0.19 V	0.12 V	**1.25 V**	**2.11 V**
P5-0h	0.16 V	0.01V	0.19 V	**2.72 V**	0.45 V
P5-10h	0.17 V	0.01 V	0.18 V	**2.30 V**	**7.14 V**
P5-20h	0.19 V	0.01 V	0.15 V	**1.76 V**	0.40 V

TABLE III
MAXIMUM VOLTAGE BOUNCE, $h = 0.254$ mm

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.47 V	0.21 V	0.49 V	0.97 V	0.49 V
P1-10h	0.53 V	0.20 V	**1.24 V**	**1.06 V**	0.84 V
P1-20h	0.63 V	0.19 V	0.32 V	0.88 V	**9.45 V**
P2-0h	0.19 V	0.46 V	0.67 V	**4.69 V**	0.81 V
P2-10h	0.20 V	0.45 V	0.81 V	**3.21 V**	**1.43 V**
P2-20h	0.20 V	0.43 V	0.12 V	**2.49 V**	**10.0 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	**1.19 V**
P3-10h	0.31 V	0.36 V	**1.17 V**	0.09 V	0.61 V
P3-20h	0.33 V	0.38 V	0.74 V	0.31 V	**13.7 V**
P4-0h	0.75 V	0.34 V	0.21 V	**3.48 V**	0.75 V
P4-10h	0.81 V	0.37 V	0.23 V	**2.57 V**	**3.94 V**
P4-20h	0.89 V	0.40 V	0.23 V	**2.08 V**	**13.3 V**
P5-0h	0.32 V	0.02 V	0.38 V	**4.96 V**	**1.03 V**
P5-10h	0.37 V	0.01 V	0.32 V	**3.64 V**	**1.04 V**
P5-20h	0.44 V	0.01 V	0.26 V	**2.89 V**	**9.39 V**

TABLE IV
MAXIMUM VOLTAGE BOUNCE, $h = 0.508$ mm

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.97 V	0.42 V	**1.21 V**	**1.68 V**	0.64 V
P1-10h	**1.17 V**	0.39 V	0.21 V	**1.76 V**	**33.8 V**
P1-20h	**1.63 V**	0.36 V	**121.5 V**	0.65 V	0.19 V
P2-0h	0.38 V	0.92 V	**1.52 V**	**8.38 V**	**1.97 V**
P2-10h	0.40 V	0.88 V	0.52 V	**5.41 V**	**41.9 V**
P2-20h	0.40 V	0.86 V	**106.8 V**	**3.26 V**	**2.08 V**
P3-0h	0.58 V	0.70 V	**1.06 V**	0.38 V	**3.63 V**
P3-10h	0.64 V	0.74 V	**1.38 V**	0.39 V	**61.8 V**
P3-20h	0.73 V	0.78 V	**45.51V**	0.45 V	0.11 V
P4-0h	**1.52 V**	0.69 V	0.44 V	**6.26 V**	**1.29 V**
P4-10h	**1.70 V**	0.76 V	0.47 V	**4.47 V**	**61.5V**
P4-20h	**2.07 V**	0.87 V	**3.74 V**	**3.82 V**	**1.24 V**
P5-0h	0.68 V	0.04 V	0.73 V	**9.02 V**	**1.99 V**
P5-10h	0.82 V	0.02 V	0.56 V	**6.20 V**	**41.5 V**
P5-20h	**1.20 V**	0.01 V	**2.09 V**	**5.22 V**	0.57 V

Tables V–VII: Plane bounce using *RC* termination, where "0h" represents no termination. R = 2 Ω and C = 20 pF (Shaded represents values >1 V bounce).

TABLE V
MAXIMUM VOLTAGE BOUNCE, $h = 0.127$ mm AND 26 *RC* TERMINATIONS

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-0hRC	0.09 V	0.04 V	0.16 V	0.19 V	0.09 V
P2-0h	0.10 V	0.23 V	0.34 V	**2.59 V**	0.41 V
P2-0hRC	0.08 V	0.26 V	0.31 V	0.38 V	0.27 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-0hRC	0.11 V	0.13 V	0.41 V	0.26 V	0.35 V
P4-0h	0.38 V	0.17 V	0.10 V	**1.91 V**	0.47 V
P4-0hRC	0.26 V	0.10 V	0.21 V	0.09 V	0.36 V
P5-0h	0.16 V	0.01 V	0.19 V	**2.72 V**	0.45 V
P5-0hRC	0.06 V	0.04 V	0.38 V	0.34 V	0.11 V

TABLE VI
MAXIMUM VOLTAGE BOUNCE, $h = 0.254$ mm AND 26 *RC* TERMINATIONS

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.47 V	0.21 V	0.49 V	0.97 V	0.49 V
P1-0hRC	0.06 V	0.10 V	0.10 V	0.28 V	0.30 V
P2-0h	0.19 V	0.46 V	0.67 V	**4.69 V**	0.81 V
P2-0hRC	0.12 V	0.27 V	0.10 V	0.44 V	**1.15 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	**1.19 V**
P3-0hRC	0.15 V	0.32 V	0.05 V	0.07 V	0.92 V
P4-0h	0.75 V	0.34 V	0.21 V	**3.48 V**	0.75 V
P4-0hRC	0.38 V	0.35 V	0.40 V	0.81 V	0.79 V
P5-0h	0.32 V	0.02 V	0.38 V	**4.96 V**	**1.03 V**
P5-0hRC	0.03 V	0.12 V	0.22 V	0.70 V	0.51 V

TABLE VII
MAXIMUM VOLTAGE BOUNCE, $h = 0.508$ mm AND 26 *RC* TERMINATIONS

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.97 V	0.42 V	**1.21 V**	**1.68 V**	0.64 V
P1-0hRC	0.26 V	0.02 V	0.06 V	**1.03 V**	**2.10 V**
P2-0h	0.38 V	0.92 V	**1.52 V**	**8.38 V**	**1.97 V**
P2-0hRC	0.13 V	0.10 V	0.53 V	0.57 V	**3.66 V**
P3-0h	0.58 V	0.70 V	**1.06 V**	0.38 V	**3.63 V**
P3-0hRC	0.15 V	0.23 V	**1.08 V**	**0.96 V**	**1.71 V**
P4-0h	**1.52 V**	0.69 V	**0.44 V**	**6.26 V**	**1.29 V**
P4-0hRC	0.37 V	0.47 V	**1.89 V**	0.99 V	**1.96 V**
P5-0h	0.68 V	0.04 V	0.73 V	**9.02 V**	**1.99 V**
P5-0hRC	0.09 V	0.10 V	0.27 V	**1.06 V**	**2.58 V**

The x-H rule is not as effective as *RC* termination under certain configurations, since both methodologies provide different edge termination impedance based on frequency and distance spacing between the planes.

V. RESULT #3: DIFFERENT FREQUENCIES

Three different stimulus frequencies are now provided simultaneously with one at each source location to determine maximum phasing effects at the five observation points (see Table VIII). Only the distance spacing of 0.127 mm is shown, as other configurations were almost identical in value. Voltage levels greater than 0.5 V are highlighted within the table.

TABLE VIII
MAXIMUM BOUNCE WITH THREE DIFFERENT STIMULUS SOURCES SIMULTANEOUSLY, $h = 0.127$ mm

Obv. Point	S1 (0.3GHz) S2 (0.6GHz) S3 (0.9GHz)	S1 (0.6GHz) S2 (0.9GHz) S3 (1.5GHz)
P1-0h	0.49 V	0.31 V
P1-10h	**0.62 V**	0.39 V
P1-20h	**0.63 V**	0.14 V
P2-0h	0.25 V	0.44 V
P2-10h	0.36 V	0.48 V
P2-20h	0.37 V	0.39 V
P3-0h	0.21 V	**0.50 V**
P3-10h	0.14 V	**0.53 V**
P3-20h	0.40 V	**0.82 V**
P4-0h	0.08 V	0.44 V
P4-10h	0.08 V	0.46 V
P4-20h	**0.87 V**	0.62 V
P5-0h	0.34 V	0.27 V
P5-10h	0.34 V	0.26 V
P5-20h	0.33 V	0.42 V

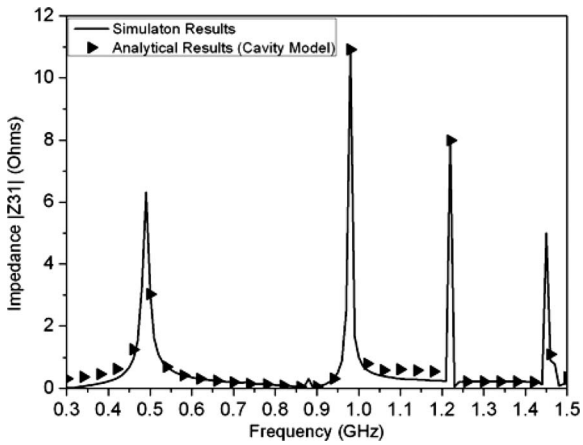

Fig. 2. Validation of plane impedance using two methods.

VI. VALIDATION OF SIMULATED DATA

To validate simulated results, we examine a single current source (1A) at port *S*1 and the observation point at *P*3. A rectangular air box enclosing the PCB implements radiation boundary condition.

Fig. 2 details numerical results using two simulation methods. Analytical results may also be obtained for this configuration using a formula provided in [7], identified by triangles in the plot.

VII. ANALYSIS: TEST DATA ANOMALES

When performing simulation, we must analyze multiple configurations along with varying parametric values to determine *if what observed falls into the realm of anticipated probability*.

To explain why large bounce values are present in simplistic terms, we excite the PDN at *S*1 using ideal current source I_1, with voltage response V_3 at *P*3 as follows:

$$V_3 = Z_{31}/I_1 \,(\text{ohms}). \tag{1}$$

From Fig. 2 at 0.98 GHz, for example, the $|Z_{31}|$ impedance is approximately 11Ω. Exciting *S*1 with a 1-A current source, the voltage response (magnitude) at *P*3 is 11 V. This large voltage value exists because plane impedance is a complex number derived from interactions in three axes and varies depending on physical location and dimension.

Since PDNs exhibit a complex and interdynamic impedance, anomalies may occur in a real product. The data herein illustrate a *theoretical situation*. This does not necessarily signify that plane bounce in excess of a volt or more will be present in an actual design.

Within a typical PCB, there are generally hundreds, if not thousands, of proagating waves being reflected back into the middle of the board from the physical edges due to numerous components switching logic states simultaneously. Phasing of multiple signals could result in deterioration of power integrity if propagating waves are in phase addition.

Results may seem unreasonable, but acceptable, if explained using appropriate mathematics to ensure the analysis is solid.

VIII. Solution—Preventing Plane Bounce

Decoupling capacitors pull the impedance of a PDN down to a small value, usually about 1 Ω or less, but *only* within a limited bandwidth of operation and generally within a narrowly observed topology of the board limited by the equivalent series resistance (ESR) and dynamic impedance of the devices used in the assembly. If cross-conduction currents are far less than 1 A, typically 1/100 or 1/1000 of 1A, and using (1), $|Z|$ will be significantly less than 1 Ω along with corresponding plane bounce and SSN.

IX. Conclusion

Power and return planes, or the PDN, function identical to signal transmission lines that are electrically long and require termination. The only difference between the two is scaling. If an unterminated transmission line exists, reflected waves back to the source will occur from the physical edge of the PCB. Phasing of reflected waves can cause functionality problems if the impedance of the PDN is high at a specific location within the layout.

Prior research used only a single stimulus source. It was shown that using multiple stimuli, the same effects will be observed as published in numerous references, except that the magnitude of plane bounce will be significantly greater if a low-impedance PDN along with use of decoupling capacitors is not provided.

A designer should at least be conceptually aware about the production of resonant frequencies and phasing effects (additive or subtractive) before beginning full board-level simulation. This is in addition to how each stimulus source behaves based upon multiple source frequencies and their physical location where they are developed. Decoupling (storage) capacitors interact dynamically with these planar effects and ensure functional operation.

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