Analysis on Loop Area Trace Radiated Emissions from Decoupling Capacitor Placement on Printed Circuit Boards

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ABSTRACT

This paper presents, with a solid conclusion, practical, hands-on applied EMC information for engineers that can be put to immediate use without relying on the mathematics of Maxwell's equations. An examination is made to determine if the physical placement of decoupling capacitors makes a significant difference in the development and propagation of radiated emissions from a printed circuit board (PCB) when used with *actual*, high-speed components. The focus is on what happens on both the top and bottom layers of a PCB, regardless of whether the board is single-sided, double-sided or multilayer. This paper complements existing research that investigates decoupling using simulation. Correlation between simulation and actual results is supported in this paper.

A problem with simulation is that results calculated sometimes cannot take into consideration common-mode RF energy developed by components switching multiple outputs under maximum capacitive load, consuming a large amount of inrush current or impulse currents from switching cross-conduction. Common-mode energy cannot always be efficiently simulated at this time, thus causing the possibility of inaccurate assumptions regarding anticipated radiated emissions from a PCB layout.

Behavioral models used for simulation are usually (theoretically) perfect and may not represent actual design parameters due to parasitics and other electromagnetic effects that cannot be easily calculated or anticipated. RF energy is developed due to digital components switching logic states. A voltage gradient on the power and ground planes between components causes common-mode EMI to be observed on interconnects and other radiating structures. Decoupling capacitors are provided to minimize voltage gradients, along with minimizing RF switching energy injected into the power distribution network and distributed throughout the entire PCB. The magnitude of radiated energy, related to decoupling capacitors is investigated in this paper, based on the physical location to digital components. In addition, common engineering problems in determining an optimal decoupling capacitor value are presented, with regard to both time and frequency domain analysis.

INTRODUCTION

Significant research and simulated results on the efficiency of decoupling capacitors to minimize radiated emissions have been published, related to decoupling capacitors and multilayer PCBs [3, 4]. Conclusions deal mainly with the magnitude of the impedance provided by the capacitor. In addition, the effect of multiple capacitor usage and self-resonant frequency anticipated was investigated. Analysis was performed without components, which may not represent what can really happen in a real product design due to parasitics. In addition, the need to minimize lead-length inductance was emphasized, which is the most important aspect for decoupling, validated and re-examined herein.

Theory and mathematical analysis allows one to understand the mechanism of what is happening within the PCB. This type of research generally becomes questionable when applied to an actual design, hence the need to validate analysis with a real product. Fast transient inrush surges cause ground bounce and voltage drop, or change in the power and ground system, at switching frequencies. Board level induced noise affects other components on the PCB, creating a voltage gradient. This voltage gradient causes common-mode energy to be developed [1, 2, 5, 6]. Using active components provides insight on what really happens in a PCB, instead of theoretical analysis based on the mathematics of simulation software. The reason for this is that the simulation engineer may use an incorrect topology layout, inaccurate behavioral models or assumptions that do not correlate to the final design, including the driver's actual output parameters. Consideration is sometimes not made on how PCBs are designed or manufactured, due to lack of parametric data and tolerances within the manufacturing process. Simulation may overly simplify problems related to actual circuit operation.

Items investigated herein, besides the magnitude of emissions from the loop area of a decoupling capacitor, includes selection for self-resonant frequency and amount of energy storage capacity. All three items must be considered when selecting a capacitor to minimize effects of board level induced noise and development of common-mode radiated RF energy.

TEST ENVIRONMENT AND SETUP

A simplified schematic of the test PCB is shown in Figure 1. A 74FCT244 was used based upon extreme operating parameters for which this device is designed. This component has a large output voltage drive level (+5V CMOS), fast edge transition rate and large inrush current consumption. Clock signals at different frequencies is applied to all eight input gates simultaneously, stressing the component to maximum operating parameters. The output of each driver has a resistive/capacitive load (47pF / 47Ω). When all gates switch simultaneously, a maximum inrush of 960 mA was anticipated. In reality, 380 mA was the total amount consumed under maximum capacitive load. The resistor/capacitor combination was connected directly to each output, separated only by a single via through the board. Radiated emissions from output traces were thus removed from the analysis due to a maximum trace length of 0.062 inches (1.6 mm).

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Provisions for six decoupling capacitors were made for the topologies detailed in Figure 1. One configuration has a capacitor (C16) located immediately adjacent to the input power pin as close as physically possible to minimize lead length inductance; best case PCB layout. The 74FCT244 has power on pin 20 and ground on pin 10, typical configuration of a dual inline package (DIP). Five capacitors (C11-C15) are located at a distance of 2.5, 3.0, 3.5, 4.0 and 4.5 inches (6.4, 7.6, 8.9, 10.2 and 11.4 cm) away. The value of the capacitor chosen was 3900 pF (3.9 nF). Only one capacitor was provided at a time for analysis during the first set of testing.

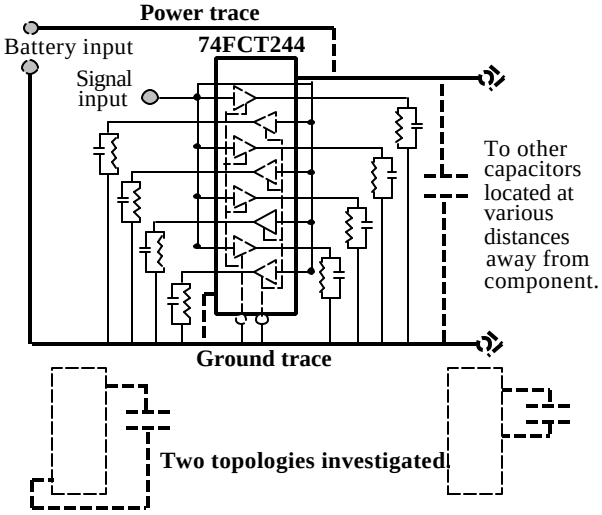


Figure 1. Simplified schematic of the test PCB.

Upon completion of the first set of measurements, the same value capacitor was installed in all locations and tested to determine overall magnitude of parallel decoupling. Three different capacitance values were investigated: 0.1µF, 3900pF and 1000pF (0.001 µF). Zero ohm resistors were used to extend the length of the decoupling loop. These resistors prevented having an unterminated stub on the load side of the decoupling capacitor. An insignificant amount of lead length inductance to the decoupling loop was observed from the resistors. The reason why lead-length inductance from these resistors could be disregarded is that the amount of equivalent series inductance (ESL) from the zero ohm resistors was *magnitudes* less than the total impedance of the 0.010 inch (0.25 mm) wide power and ground trace. Ferrite beads prevented switching noise corruption to the power source.

Radiated emissions were measured in a TEM cell. A battery internal to the TEM cell provided +5 VDC, thus minimizing switching noise effects from a power supply. A digital clock signal was injected to the test PCB from an external source through a SMA connector. Ferrite clamps minimized influences of the signal cable entering the TEM cell, ensuring that the signal was greater than 40 dB below the emissions measured from the test PCB. The reason to not provide on-board clock generation was to allow measurement of *actual* emissions from the 74FCT244 by itself, along with the effects from various decoupling loop areas; not from a frequency generation source. A total of forty plots were taken. Only significant data is presented herein, illustrating the magnitude of the emissions from various configurations. Specific frequencies of 10.00, 42.00 and 80.00 MHz were provided for all configurations.

FREQUENCY DOMAIN ANALYSIS

The reason 3900 pF capacitors were chosen for this experiment is due to how a typical design engineer would, theoretically, specify a decoupling value. The 74FCT244 was chosen to be used with an 80 MHz input signal. This frequency would stress the component to near maximum operating parameters. The self-resonant frequency of a capacitor at 80 MHz, with typical lead inductance (ESL) of 1-nH (0805 surface-mount package size) calculates to be 3900 pF per Eq. (1). This capacitor selection value proved to be an interesting choice, discussed later.

$$f = \frac{1}{2\pi\sqrt{LC}} \tag{1}$$

Total inductance of the decoupling loop includes the trace distance from the power pin to the capacitor and trace distance from the ground plate of the capacitor to the component's ground pin. For a DIP package, a very long trace length is always present due to physical dimensions of the layout, regardless of the actual location where the capacitor is placed, typical of board designs without power and ground planes. The new, self-resonant frequency, *f*, of the decoupling loop is recalculated per Eq. (1) using the value of 3900 pF, chosen for its operation at 80 MHz, the desired test frequency. The new value of inductance, *L*, for the equation is now *both* the equivalent series inductance (ESL) of the capacitor *and* the interconnect trace, detailed in Table 1.

Parametric values for all decoupling configurations, using a routed trace width of 0.010 inches (0.25 mm), chosen for its ability to handle 1.5 amps of DC current follows. This trace width has an impedance of approximately 131 ohms (referenced to the ground plane on the bottom of the assembly). Trace inductance is 18-nH/inch (7-nH/cm), and lumped capacitance Co is 1.06 pf/inch (0.42 pf/cm). The variable *L* represents total inductance (H) while *C* is capacitance (F). Tolerance of the capacitor is ± 10%. The total distributed capacitance of the decoupling loop is magnitudes *less* than the value of the discrete capacitor (3900 pF or 3.9 nF). Hence, this distributed capacitive value can be disregarded for calculations related to decoupling capacitor placement.

Radiated emission, *E* (µV/m) expected from the loop area between capacitor and component is determined by Eq. (2) [7]. Loop area ($A=\pi r^2$) is determined by extracting the radius from the known loop perimeter, *C*, ($C=2\pi r$). Current draw is 380 mA, under maximum load conditions. The variables in Eq. (2) involve *A* = loop area (cm^2), *I* = current (mA), *f* = frequency in MHz, and *r* = distance between loop and measuring antenna (meters). For purpose of the calculation, a measurement distance of 3 meters is used to represent FCC Class B limits. It is noted that specification limits for FCC above 1 GHz do not exist at this time for certain types of unintentional radiators. Table 1 also describes Eq. (2). The emission levels are very low, based on a small loop structure.

$$E = \frac{Af^2 I}{380r} \tag{2}$$

Equation (3) calculates the wavelength of a propagated signal. This wavelength is related to the total loop perimeter from capacitor placement, forming a radiating structure, with *f* = frequency (MHz), and *l* = wavelength in meters. This is the frequency in which the loop area becomes an efficient antenna.

Table 1. Parametric Details of the Test PCB.

Capacitor ID	Loop perimeter due to capacitor placement	Total loop inductance [1]	Self-resonant frequency of the loop path[3]	Calculated emission levels @ 10 MHz[4]	Calculated radiated frequency (loop area)[5]
C11	2.5 inches (6.4 cm)	46 nH	11.5 MHz	108.8 µV/m	4.8 GHz
C12	3.0 inches (7.6 cm)	55 nH	10.8 MHz	153.4 µV/m	3.9 GHz
C13	3.5 inches (8.9 cm)	64 nH	10.0 MHz	210.3 µV/m	3.4 GHz
C14	4.0 inches (10.2 cm)	73 nH	9.4 MHz	276.3 µV/m	2.9 GHz
C15	4.5 inches (11.4 cm)	82 nH	8.9 MHz	345.1 µV/m	2.6 GHz
C16	0.01 inches (0.25 mm)	3.18 nH [2]	45.2 MHz	0.17 µV/m	1,200 GHz

1. Includes package lead-length inductance (1-nH) and trace inductance from the total loop area (18 nH/inch).
2. Inductance value contains lead-length inductance (1-nH) and one via (2-nH).
3. Value of capacitor used for calculating self-resonant frequency, Eq. (1): 3900 pf (3.9 nF) and total loop inductance, *L*.
4. Distance used is 3 meters, calculated from Eq. (2).
5. Loop area determined from loop perimeter for use with Eq. (3).

For a 10 MHz test signal, one wavelength (λ) = 30 meters. At 10 MHz, one-twentieth of a wavelength (λ/20) = 1.5 meters. Consequently, the loop area from decoupling capacitor placement on the PCB, being very small, cannot become an efficient radiating loop antenna. The test data and plots confirmed this.

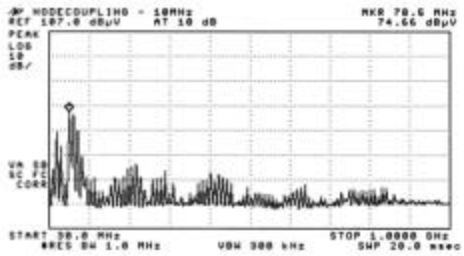
$$f = \frac{300}{\lambda} \tag{3}$$

The magnitude of all configurations, related to radiated emissions due to the decoupling loop area was nearly identical, regardless of physical placement. Equation (3) shows the frequency that should be observed as a result of differential-mode RF energy developed by the decoupling loop. This frequency is well into the GHz range. In addition, the magnitude of radiated energy and corresponding frequency can be mathematically calculated and measured. *The physical location of a decoupling capacitor, which allows a loop area to exist, does have an effect on radiated emissions.* Plots indicate that although classic equations exist to calculate emissions and anticipated frequency, these equations are valid only under absolute conditions – no components provided. Parasitics elements cause emissions to occur at magnitudes greater than the component itself and at frequencies not expected.

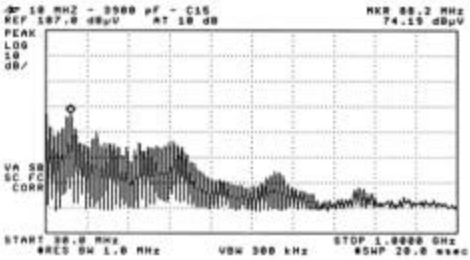
Analysis of the data, including plots not provided herein, indicates regardless of physical placement on the PCB, decoupling effects are observed, with radiated emissions present. Emissions from the component were expected to be magnitudes greater without decoupling capacitors than with. This was an interesting revelation, shown in Figure 2. Amplitude levels of all decoupling locations were nearly identical; spectral shifts were noted. The size of the loop area thus *did not* have a significant effect on the magnitude of radiated emissions for different capacitor locations.

Radiated emissions are due to a combination of transient switching currents, shaped by other parasitics within the circuit. These parasitics include the manufacturing process of the silicon wafer, and a higher impedance value from the package bond wires over that of wide PCB traces that provide power and ground. Current consumed by the circuit increases due to the lower impedance caused by the addition of a capacitor.

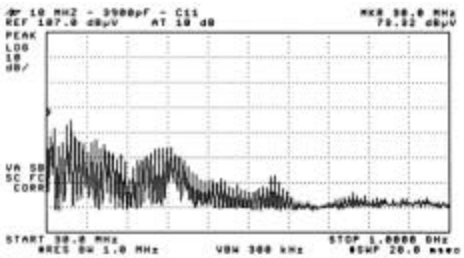
The real reason why the decoupling loop radiates RF energy is explained by [6]. The power and ground structure is differential-mode. Differential-mode voltage or currents results in common-mode current being established on an attached cable, in this case a PCB trace. A dipole antenna is now created by the existence of the decoupling loop, with the driven element the voltage rail and ground as the other side of the antenna. When a capacitor is installed at the end of a dipole antenna, RF energy travels through the capacitor. The capacitor's dielectric emulates free space, allowing common-mode current from the device to drive the capacitor (antenna). This concept is illustrated by Figure 3.



No decoupling – 10 MHz.



Worst case decoupling, 3900 pF – 4.5" away, 10 MHz.



Typical decoupling location, 3900 pF – 2.5" away, 10 MHz.

Figure 2. Radiated emissions from sample loop areas.

As the physical dimension of the decoupling loop becomes smaller, the frequency at which radiated energy exists increases

into the Gigahertz range. At such high frequency, well above most concerns related to compatibility with certain categories of electronic equipment, should engineers incorporate layout techniques to prevent propagation of unintentional RF energy?

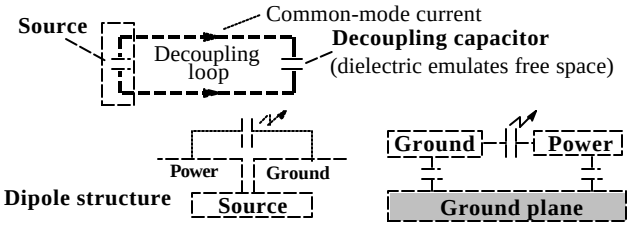
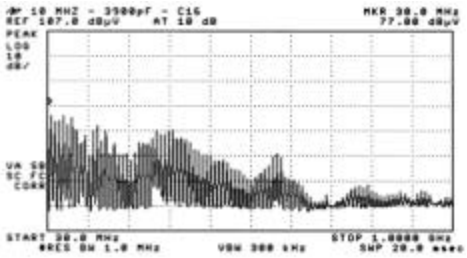


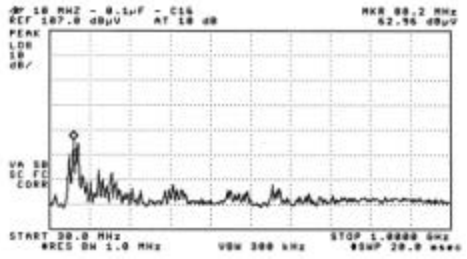
Figure 3. Antenna structure due to decoupling placement.

The spectral distribution of propagated energy is based on the minimum edge rate transition of a digital component. This frequency is generally so high that the issue of loop area for decoupling capacitors becomes moot for the majority of product designs. A greater concern should be placed on minimizing board level induced noise voltage, ground bounce and production of common-mode RF energy.

The theoretical, self-resonant frequency of a 3900 pF, surface mount capacitor (0805 package size), with lead length inductance of 1-nH is 80 MHz. This self-resonant frequency is valid only if the capacitor *is never installed* on the PCB. When installed, the actual, self-resonant frequency becomes the value in Table 1, decreasing from 80 MHz to as low as approximately 10 MHz.



Minimum loop dimension possible, 3900 pF – 10 MHz.

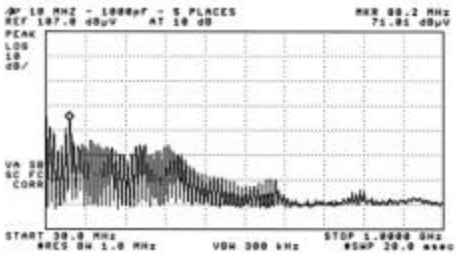


Minimum loop dimension possible, 0.1 µF - 10 MHz.

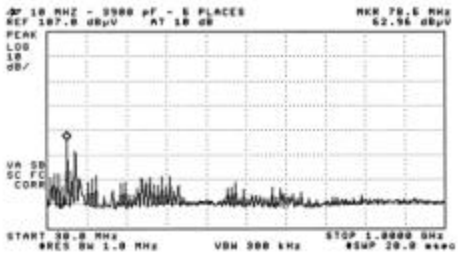
Figure 4. Effect of different capacitor values, same location.

Many design engineers overlook the magnitude of change in resonance when specifying the value of a decoupling capacitor, based on actual trace inductance. Radiated emissions were now measured with a different capacitance value, at the same operating frequency, to determine any effects. Figure 4 shows replacing the 3900 pF capacitor (chosen because it was supposed to be self-resonant at 80 MHz, the desired test frequency), with a 0.1 µF capacitor. The 0.1 µF capacitor is self-resonant at 16 MHz, based on actual trace inductance. The 3900 pF capacitor, located in this best-case physical position (C16), is resonant at 45 MHz. When provided in locations C11-C15, the 3900 pF capacitor is resonant at approximately 10 MHz.

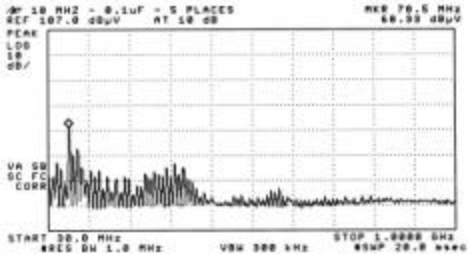
If physical placement has no effect on emissions, then why did a significant reduction in radiated energy occur? The magnitude of radiated emission reduction was due to a *greater amount of stored energy charge* provided by the 0.1 µF capacitor, not the loop area dimension. The 0.1 µF capacitor charges and discharges at nearly the same frequency as the device. The 3900 pF capacitor, with limited energy storage (operating at 45 MHz), could not provide sufficient energy to the component due to its small capacitive value. Figure 5 illustrates the effects of five decoupling capacitors in parallel, all with the same value. The net effect is that all capacitors charge and discharge at approximately the same frequency, however, the total amount of energy to the 74FCT244 is five times larger. The greater the charge energy, at the operating frequency of the device, a reduction in radiated emission will occur. *Reduced emissions occurs because the differential-mode balance of the power and ground structure is enhanced.*



Five capacitor – 1000pF (0.005 µF total) – 10 MHz.



Five capacitor – 3900pF (0.02 µF total) – 10 MHz.



Five capacitor – 0.1 µF (0.5 µF total) – 10 MHz.

Figure 5. Magnitude of emissions - multiple capacitors.

With use of parallel decoupling, lead length inductance is reduced inversely to the number of capacitors provided. This inductance reduction is magnitudes *less* than the inductance of the loop

structure of all trace and bond wires. The magnitude of inductance reduction from parallel capacitors can be ignored for most purposes of analysis, due to magnitude of scale.

As a capacitor charges and discharges, it does so at a specific frequency. If the component performs several clock cycle operations during a single charge/discharge period, ground bounce and induced noise into the power and ground structure becomes a greater concern then EMI. The key item for enhanced EMI performance, and signal integrity, is to *not* use a trace between capacitor and component. Use a via directly to the power and ground planes, if provided. This configuration minimizes loop inductance for a multilayer stackup assembly [4].

TIME DOMAIN ANALYSIS

Research [3, 4] shows that a lumped model can be used to describe a power and ground plane structure. This lumped model is common with multilayer PCB analysis. The model assumes that sufficient decoupling to components up to several hundred MHz occurs. The physical placement of a decoupling capacitor, (within reason), is not critical, as energy charge is distributed in a radial fashion to all components located in the vicinity of the capacitor. Energy to components travel at a propagation speed dependent on the dielectric constant of the planar material, which is generally magnitudes faster than the edge transition time of most digital components, at the present time.

The velocity of propagation of energy within a transmission line (PCB trace) or plane is dependent exclusively on the dielectric constant of the material. For the worst case loop dimension on the PCB, 4.5 inches (11.4 cm) microstrip topology, propagation delay is 1.72 ns/ft (0.36 ns/cm). This value is based on a dielectric constant, ε_r = 4.6, ($t_{pd} = 1.017\sqrt{0.475\varepsilon_r + 0.67}$). This calculation illustrates that the decoupling capacitor can be located a significant distance away (time domain analysis) from the component and provide charge long before the next edge transition event occurs. With this configuration, it takes the charge energy approximately 21% of the time period available to reach the component. If the capacitor is physical closer, energy will be received at the device in less time, which is desirable.

A switching event causes a large amount of inrush current from the power distribution network, causing a voltage or ground potential difference between components. Although the power distribution network provides sufficient charge storage for certain designs, a finite time period exists when the power and ground network is unable to operate efficiently. This finite period is due to logic crossover between transition states from the gates internal to the silicon wafer. If power and ground is provided to components by traces, not planes, typical of single- and double-sided PCB designs, a significant functionality concern develops. This concern deals with component level induced noise into the power distribution system, affecting operation of other devices throughout a distributed structure.

Simulated analysis of placing decoupling capacitors anywhere on the PCB is accurate, as long as no components are provided. Enhanced decoupling is observed when the capacitor is connected to planes by vias. In reality, locating a capacitor anywhere on the PCB is not desired from a layout viewpoint. If traces are to be routed for power and/or ground between capacitor and device (includes pin escapes and breakout from the device pin to a via for interconnect to another layer; power or ground) trace inductance exists. The inductance from traces will lower the self-resonant frequency of the capacitor. This reduction permits a voltage-gradient to be present in the power distribution network. This voltage-gradient is one cause in the development of common-mode energy. The impedance of planes is magnitudes less than a trace. Low planar impedance is the reason why planes work as well as they do. The problem with a real PCB is that not every design will have planes available, and in many cases, traces may have to be provided, regardless of stackup assignment.

Power and ground planes are assumed to provide sufficient energy storage to minimize use of discrete capacitors. Simulation of simple structures cannot accurately calculate actual storage capacity required, and the ability of the capacitor to minimize board level induced noise when many components switch logic states simultaneously under maximum capacitive load. Equation (4) illustrates amount of stored energy required for minimizing induced noise voltage. Minimum decoupling capacitance required is determined by Eq. (5).

$$Q = CV \quad (Coulombs) \tag{4}$$

$$C = \frac{dI\ dt}{dV} \quad (A) \tag{5}$$

Board induced noise voltage was measured, Table 2, for various capacitor placement locations. When multiple capacitors are provided in parallel, the total capacitance increases in direct proportion to the number of components provided. The self-resonant frequency of all parallel capacitors will be nearly identical. As the amount of stored energy increases, board level power or ground induced noise will decrease, enhancing signal integrity and functionality. Table 2 validates the need for sufficient stored energy charge from the decoupling capacitor(s). *Board level induced noise is one cause of radiated emissions.* Capacitors must provide sufficient energy at switching frequencies (self-resonant value) in addition to minimizing induced noise voltage in the power distribution system.

The interesting item to note is that regardless of physical placement of a decoupling capacitor, from best to worst case location, C11-C15 (2.5 inches to 4.5 inches), board level EMI amplitudes measured was nearly identical. This identical value was due to the same approximate amount of energy charge being providing to the component, regardless of physical placement. The energy charge traveling from the decoupling capacitor was well within the time period between logic state transitions.

Table 2. Time domain analysis.

Configuration	Bounce level	RF emissions
No decoupling	1.6 V	minor
C11 (3900 pF)	506 mV	maximum
C12 (3900 pF)	588 mV	maximum
C13 (3900 pF)	590 mV	maximum
C14 (3900 pF)	634 mV	maximum
C15 (3900 pF)	670 mV	maximum
(5) 1000 pF - 0.005 µF total	164 mV	moderate
(5) 3900 pF - 0.02 µF total	467 mV	minimum
(5) 0.1 µF - 0.5 µF total	506 mV	moderate

In order to ensure functionality, the supply voltage level cannot drop more than 250 mV during an edge transition. The measured

voltage drop greatly exceeded 250 mV. The vendor data sheet does not specify what the edge rate transition is. Typically, this logic family is specified at 1-2 ns. In reality, the actual, measured edge transition of the 74FCT244 is 0.8 ns. This unpublished specification is a primary cause of signal integrity concerns, in addition to the development of EMI.

Minimizing board level induced noise decreases radiated emissions. Less common-mode energy is now present between a driven source and a secondary element, or load. For the test PCB, the secondary element is the antenna structure of the decoupling loop, acting as a driven antenna [6]. The plots in Figure 5 illustrate the effects of increased stored charge energy using multiple capacitors with the same capacitive value.

A typical power and ground distribution network cannot provide significant energy to certain devices within a very small time period, in this case, 0.8 ns. Consideration must be made during the design cycle for *all* devices provided within a PCB assembly, not just one component typically investigated with a simulation program. Many devices switch logic states synchronously, which places a strain on the power supply and power distribution network. The power supply cannot respond fast enough to replenish the power and ground network due to a typically high impedance value of the interconnect between the power supply and PCB. In addition, the power supply generally contains very large electrolytic capacitors on the output to minimize ripple and power dropout. These capacitors cannot replenish charge to a PCB to at switching frequencies, common in today's products.

CONCLUSION

Radiated emission from use of decoupling capacitors is both a time domain and frequency domain issue.

Frequency domain analysis. The dimension of a decoupling loop, due to capacitor placement, plays a minor role in the amplitude development and propagation of RF emissions. The perimeter of the loop emulates a dipole antenna, radiating common-mode energy. The capacitor acts as the driven portion of the antenna structure, due to an imbalance in the differential-mode power distribution network. Once a capacitor is applied to a PCB, the calculated self-resonant frequency decreases significantly, minimizing effectiveness of the capacitor due to excessive lead-length inductance. A very small loop does not generate any greater magnitude of radiated emissions than a capacitor located further away, although spectral shifts are observed.

Time domain analysis. It was determined, using an active logic device operating under maximum capacitive load, switching transition states, that board level induced power or ground noise is one cause of radiated RF emissions. Board level induced noise is difficult to simulate, as numerous parasitic parameters are not available in behavioral model form. These parameters include the amount of common-mode radiated emissions from the silicon wafer die inside a plastic enclosure, type of manufacturing process of the silicon, input/output buffer behavioral models, actual construction of the PCB, external transmission line interconnects and power distribution purity. Classic methods for selection of a decoupling capacitor are now partially ineffective for optimal prevention of noise in the power and ground structure, in addition to reducing radiated emissions and minimizing board level noise voltage.

Summary. The following is a recommended method of selecting a capacitor to reduce emissions and minimize board level noise.

Connect decoupling capacitors directly to the power and ground planes by vias [3, 4, 8]. Vias are preferred over traces due to significantly less lead length inductance. Selection of a decoupling capacitor must be made by first determining maximum amount of charge required to minimize bounce, Eqs. (4) and (5), based on actual operating parameters (maximum capacitive load), not historical data or past design rules. Follow this calculation by next determining self-resonant frequency, Eq. (1), or actual switching speed of the component and capacitor. Calculate or measure the real loop inductance, including those in the lead frame of the component package.

Manipulate the value of capacitance for a specific self-resonant frequency, using actual inductance of the loop perimeter, while maintaining summation total for desired storage capacity. The lead-length inductance of a capacitor is generally *magnitudes* less than total trace inductance.

ACKNOWLEDGMENT

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