Printed Circuit Board Design Techniques for EMC Compliance (One or Two Day Seminar)

Introduction

This course stresses hands-on techniques related to the design and layout of printed circuit boards. Basic signal integrity and the theory of electromagnetic compatibility (EMC), along with regulatory compliance requirements are presented. This introductory course was developed for both junior level and new engineers to the field of EMC, introducing them to basic concepts of proper printed circuit board design techniques.

The participant, upon completion, should be able to create or locate problems on a high-density, high technology printed circuit board with minimal difficulty. With proper implementation of the techniques presented, one should meet or exceeds test and system level requirements during the first revision of any design. Layout techniques of years past are now insufficient to address today's technology products for both signal integrity and EMC.

In an informal atmosphere, design and layout techniques are introduced in an easy to follow step-by-step presentation that allows plenty of opportunities to address specific questions. Instructional emphasis is placed on real-life examples that demonstrate good layout practices that can be incorporated immediately into any design. For this course, please bring in artwork and schematics to analyze (existing or obsolete) for design flaws (electronic media only). This essentially makes this a unique course that addresses the interest of the student and not what the instructor believes what the attendees want to hear.

Course Objective

This course presents both simplified theory and "rules-driven, hands-on techniques" for minimizing the development of EMI developed and propagated within a printed circuit board. The focus is at the *fundamental* level. Rigorous mathematical analysis and theory will *not* be presented. The seminar is geared toward multi-layer, high-density designs. Requirements for single- and double-sided designs are examined based upon fundamental concepts for multi-layer boards.

The objective is to allow engineers to understand how a PCB functions with transmission lines between components, how RF energy is created, and to provide insight into concepts and tools that assist in optimizing a design during the layout and debug cycle. Proper layout not only assures functionality, but also compliance with EMC requirements plus compatibility between electrical systems to ensure operation for the life of the system for both commercial and military applications.

The discussion on EMC, which is a major part of this course, is based on implementing RF suppression at the printed circuit board instead of relying on system level containment for emissions and immunity.

Who Should Attend

This course is intended for *practicing* design engineers of all disciplines, regulatory compliance engineers, EMC consultants and PCB designers. No formal training in electronic theory is required. Concepts, theory and layout techniques are presented in an easy to understand format, *without math*, using practical and real world examples. Engineers, technicians, supervisors and managers will also gain valuable insights into PCB design and layout for today's high technology products along with obstacles that exist for the designer.

Benefits of Attending

- Increased job knowledge
- Enhanced signal integrity and EMC compliance
- Teaches EMC suppression versus containment
- Allows first-time compliance to EMC requirements
- Reduce design time and manufacturing costs
- State-of-the-art design and layout techniques presented

About the Instructor

Mark Montrose is principle consultant of Montrose Compliance Services, Inc., a full service regulatory compliance firm specializing in Electromagnetic Compatibility with 30 years of applied EMC experience. Prior to becoming a consultant, Mark was responsible for regulatory compliance for several high-technology companies in Silicon Valley, California. His work experience includes design, test and certification of both Information Technology (ITE) as well as Industrial, Scientific and Medical products (ISM). He is assessed by a European Competent Body to perform CE compliance approval and in situ testing and certification of industrial products.

Mark is a Senior Member of the IEEE and a past member of the *Board of Directors* of the IEEE as Division VI Director (2009-2010). He is also a long-term past Board member of the IEEE EMC Society plus Champion and First President of the IEEE Product Safety Engineering Society. He was a popular distinguished lecturer for the IEEE EMC Society and is considered an expert in printed circuit board design and system level applications for EMC compliance. He has presented numerous papers based on sophisticated research related to printed circuit boards and the field of EMC at International EMC Symposiums and Colloquiums worldwide. Mark also provides personalized in-house seminars and consulting services to corporate clients worldwide in addition to the University of California, Santa Cruz extension program.

Mark has authored the following best-selling text/reference books published by Wiley/IEEE Press.

- *Printed Circuit Board Design Techniques for EMC Compliance*, 1996-1st ed / 2000-2nd ed.
- *EMC and the Printed Circuit Board - Design, Theory and Layout Made Simple*, 1999.
- *Testing for EMC Compliance – Approaches and Techniques*. 2004.
- Contributing author to the *Electronics Packaging Handbook*, Chapter 6, 2000 (CRC/IEEE Press).

Montrose Compliance Services, Inc.
Electromagnetic Compatibility and Product Safety

2353 Mission Glen Drive
Santa Clara, CA 95051-1214
☎ and FAX (408) 247-5715
mark@montrosecompliance.com

Printed Circuit Board Design Techniques for EMC Compliance (One Day Version)

Fundamentals of EMC
- Definition of EMC Terms
- Classification of ITE and International Requirements
- Understanding the Frequency Spectrum and Signals
- Basic Aspects of EMC
- The EMC Environment
- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Closed Loop Circuits
- Radiated Emissions from a Closed Loop Circuit
- Return Current Path of Travel-Multilayer Assembly
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- The Need for Flux Cancellation
- Causes of EMC – System Level

Basic EMC Suppression and Grounding Concepts
- Grounding Hierarchies and Types of Grounds
- Radial Migration
- Image Plane Theory
- RF Current Retrun and Flux Cancellation
- RF Current Density Distribution
- Primary Grounding Methodologies
- Functional Partitioning
- Components Selection Related to EMC

Impedance Control of Transmission Lines
- Microstrip and StriplineTopologies
- Impedance Control Equations
- Capacitive Loading

Layer Stackup Assignments
- Single, Double and Multilayer Assignments
- Film and Manufacturing Concerns

Computerized Simulation Analysis Performing Layer Stackup & Impedance Control

Bypassing and Decoupling (Power Distribution)
- Power Distribution Network Overview
- Capacitor Details; Types, Dielectrics, Functional Use
- Capacitors Characteristic and Self-Resonance
- Effects of Capacitors in Parallel
- Power and Ground Plane Capacitance
- Multipole Decoupling Concept
- Decoupling Radius of Operation
- The Capacitor Brigade
- Dipole Effects fromUse of Decoupling Capacitors
- Placement Recommendations
- Mounting Pad and Loop Inductance
- Burried Capacitance
- Equivalent Circuit of a PCB

Clocks and Trace Routing
- Signal Spectra (Fourier Analysis)
- Calculating Maximum Trace Length for Critical Nets
- Trace Separation and the 3-W Rule
- Trace Routing for Clocks and Signals Using Termination
- Layer Jumping
- Routing Over Split Planes
- Guard and Shunt Traces
- Ground Slots and Through-Hole Components
- Crosstalk and Layout Technique to Prevent Problems
- Localized Planes
- Trace Routing for Corners

Interconnects and I/O
- Partitioning, Isolation (Moating) and Bridging
- Image Plane or Moat Violation
- Digital and Analog Partitioning, Layout and Filtering
- Filtering and Grounding
- Common-Mode and Differential-Mode Currents
- Multi-Point Grounding (I/O Connectors)
- Video and Audio Circuits

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Printed Circuit Board Design Techniques for EMC Compliance (Two Day Version)

Fundamentals of EMC
- Definition of EMC Terms
- Classification of ITE and International Requirements
- Understanding the Frequency Spectrum and Signals
- The Decibel, Variations and Pitfalls
- Basic Aspects of EMC
- The EMC Environment
- Component Characteristics at RF Frequencies
- How Printed Circuit Boards Create EMI
- Right Hand Rule
- Maxwell's Equations
- Closed Loop Circuits
- Radiated Emissions from a Closed Loop Circuit
- Return Current Path of Travel-Multilayer Assembly
- Loop Area Between Components
- Common-Mode and Differential-Mode Currents
- The Need for Flux Cancellation
- Causes of EMC – System Level

Basic EMC Suppression and Grounding Concepts
- Grounding Hierarchies and Types of Grounds
- Radial Migration
- Image Plane Theory
- RF Current Retrun and Flux Cancellation
- RF Current Density Distribution
- Primary Grounding Methodologies
- Resonance in a Multi-Point Ground
- Aspect Ratio-Minimizing Grond Loops
- Creative Implementation – Aspect Ratio
- Ground Slots and Through-Hole Components
- Functional Partitioning
- Components Selection Related to EMC

Bypassing and Decoupling (Power Distribution)
- Defining Capacitor Usage
- Physical Representation (SPICE Model)
- Capacitor Characteristic and Self-Resonance
- Effects of Capacitors in Parallel
- Power and Ground Plane Capacitance
- Decoupling Radius of Operation
- The Capacitor Brigade
- Dipole Effects fromUse of Decoupling Capacitors
- Placement Recommendations (Various Configurations)
- Location – Power or Return Pin
- Equivalent Circuit of a PCB With Capacitors

Layer Stackup Assignments
- Single, Double and Multilayer Assignments
- Film and Manufacturing Concerns

Clocks, Impedance Control and Trace Routing
- Signal Spectra (Fourier Analysis)
- Microstrip and StriplineTopologies
- Impedance Control Equations
- Capacitive Loading
- Calculating Maximum Trace Length for Critical Nets
- Trace Separation and the 3-W Rule
- Trace Routing for Clocks and Signals Using Termination
- Layer Jumping
- Routing Over Split Planes
- Guard and Shunt Traces
- Crosstalk and Layout Technique to Prevent Problems

Computerized Simulation Analysis Performing Layer Stackup & Impedance Control

Interconnects and I/O
- Partitioning, Isolation (Moating) and Bridging
- Image Plane or Moat Violation
- Digital and Analog Partitioning, Layout and Filtering
- Filtering and Grounding
- Common-Mode and Differential-Mode Currents
- Multi-Point Grounding (I/O Connectors)
- Video and Audio Circuits

Electrostatic Discharge (ESD) Protection

Backplanes, Daughter Cards and Ribbon Cables
- Design Basics - Five Areas of Concern
- Specifying Construction Requirements
- Mechanical Concerns
- Interconnects
- Signal Routing and Terminations
- Cross Talk Concerns
- Ground Slots in Backplanes

Miscellaneous Design Techniques/Concepts
- Localized Planes
- Trace Routing for Corners
- The *20-H Rule*
- How to Select a Ferrite Device
- Grounded Heatsinks
- BNC Conectors
- Lithium Battery Circuits
- Creepage and Clearance Distances