How Decoupling Capacitors May Cause Radiated EMI

Mark I. Montrose
Montrose Compliance Services, Inc.
mark@montrosecompliance.com

Abstract–This paper analyzes effects that decoupling capacitor(s) may have on the development of radiated emissions should improper implementation on a printed circuit board (PCB) occur. This applied EMC paper is based on real-world experience and contains an easy solution to help engineers achieve compliance quickly and at low cost, without having to redesign the PCB.

Improper implementation of decoupling capacitor(s) includes: routing traces on the outer layers or using boards with or without power and return planes; excessive inductance in the decoupling loop area; lack of charge storage to replenish the power and return planes; and self-resonant frequency of the capacitor outside the harmonic spectrum of periodic signals.

We analyze the magnitude of radiated electromagnetic interference (EMI) based on physical placement of decoupling capacitors from digital components and whether distance spacing from a switching element, connected by routed traces on both the top and bottom of a PCB, makes a significant difference in the development and propagation of radiated emissions. The focus is on what occurs on a PCB, regardless of whether the board is single-sided, double-sided or multilayer.

Keywords-decoupling capacitors, trace inductance, power distribution, common-mode radiation

I. INTRODUCTION

Behavioral models chosen for simulation are usually (theoretically) perfect. Perfect models along with computational analysis may not represent an actual PCB layout due to parasitics and other electromagnetic effects that cannot be easily determined or anticipated. A voltage potential difference due to inductance of the interconnect trace from a decoupling capacitor to the power distribution network (PDN) can causes common-mode EMI to be developed and propagated from digital components.

Decoupling capacitors are required to minimize voltage potential differences and plane bounce along with RF switching energy injected into the PDN from digital components. Once switching energy is injected into a PDN, this energy will be distributed throughout the power/return network within a certain radius of operation and can cause functional disruption of circuits should the magnitude of the plane bounce exceed operational margins. The magnitude of radiated energy, related to the physical placement of a decoupling capacitor with routed traces is investigated herein.

Prior research on the effectiveness of decoupling capacitors is extensive and covers namely the effects of lead inductance and RF switching noise present within a PDN, but not radiated emissions from a routed trace between component and capacitor. Examples include [1, 2]. It is a well-known fact that a PDN must have low impedance at switching frequencies to minimize plane bounce. Plane impedance is easily calculated from loop inductance (ESL) along with lumped capacitance from discrete components. The need to minimize lead inductance is emphasized in the z-axis yet minimal research has been presented on what happens when there is excessive inductance on only one leg of a decoupling capacitor (i.e., power *or* ground-0V) [3, 4].

This paper presents what happens in a real-world PCB should a poor layout topology be implemented. Not every PCB layout designer, and in fact many digital design engineers, do not understand EMC and PCB layout requirement and create a product using a routed trace between component and decoupling capacitor(s) because it is easy to implement versus placing vias to a plane for every pin of the component and both legs of a capacitor.

Fast transient inrush surges causes a bounce condition to exist on both the voltage and 0V planes at switching frequencies. In addition to plane bounce, if insufficient capacitance is present to minimize PDN noise, the magnitude of this bounce creates common-mode currents internal to the silicon of digital components. The impedance of the internal bond wires to the package pins is extremely high upon which common-mode current is also developed. Common-mode current now has several antenna structures to radiate from; the silicon or lead bond wires or routed trace(s) to a decoupling capacitor. If there is insufficient energy charge in the PDN, a potential plane bounce in power distribution may cause common-mode current to be developed [3, 4, 5, 6]. Computational analysis may not include all parametric values, may be overly simplified, or not be well defined.

II. TEST ENVIRONMENT AND SETUP

A simplified schematic and the PCB is shown in Figs. 1 and 2 to help in describing the test setup. A 74FCT244 is chosen based upon extreme operating parameters for which this device is designed to be operated under. This component has a large output voltage drive level (+5V CMOS), fast edge transition rate and up to 960 mA data book inrush current consumption under maximum capacitive load. A clock signal at different frequencies is applied to all eight input gates simultaneously, stressing the component to maximum operating/thermal parameters. Each output driver has a maximum resistive/capacitive load (47pF/47Ω). When all eight drivers switch simultaneously, the inrush surge current was 380 mA. The resistor/capacitor pair was connected directly to each output, using a single via to minimize routed trace inductance. This routed distance was 1.6 mm (0.062 inches or 62 mils).

Provisions for six decoupling capacitors with different trace lengths were provided to analyze the magnitude of common-mode current developed internal to the component's package and to determine whether the decoupling capacitor

location would increase radiated EMI. One configuration had a capacitor (C16) located immediately adjacent to the input power pin, or best possible location. Five capacitors (C11-C15) were located at a distance of 6.4, 7.6, 8.9, 10.2 and 11.4 cm (2.5, 3.0, 3.5, 4.0 and 4.5 inches) away. A non-typical capacitor value (3.9 nF) was chosen to analyze what may occur if there is insufficient decoupling capacitance instead of a theoretically perfect 100 nF device.

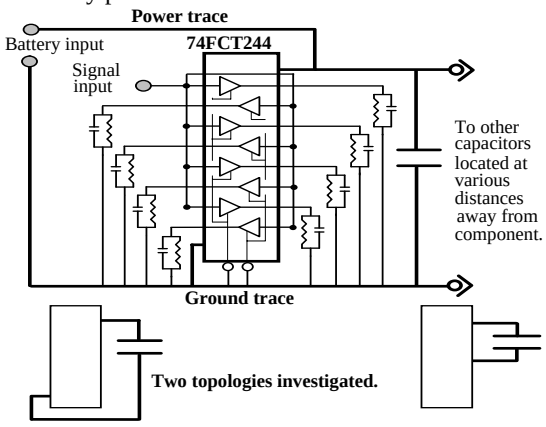


Fig. 1. Simplified schematic of the test PCB

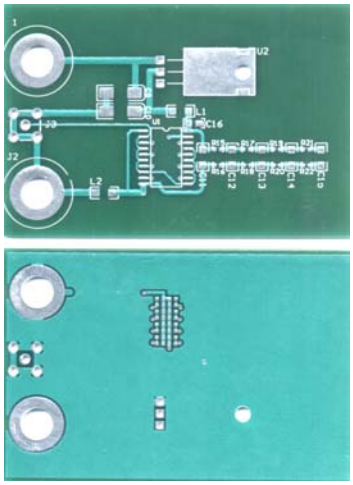


Fig. 2. PCB layout

Three different decoupling capacitance values were investigated separately and then in groups of five: 1nF, 3.9nF and 100 nF. Zero ohm resistors were used to extend the length of the decoupling loop. These resistors have a minimal amount of equivalent series resistance (ESR) and equivalent series inductance (ESL), and thus did not affect measurement results. Ferrite beads prevented switching noise corruption to/from the DC power source (battery).

An 80 MHz clock signal (maximum operating frequency of the 74FCT244) was provided using a SMA connector. The reason to not provide on-board clock generation was to allow measurement of *actual* emissions from the 74FCT244 by itself, along with the effects from various decoupling loop areas; not from a radiating frequency generation source. Due to an extensive amount of data (40 plots), typical results can only be presented. The key item to observe is both cause and effects based on a many test plots and data.

III Frequency Domain Analysis

The reason 3.9nF capacitors were originally chosen is due to how a typical junior design engineer may [incorrectly] select a decoupling value without taking into consideration loop inductance. The self-resonant frequency of a capacitor at 80 MHz, with typical lead inductance (ESL) of 1nH is 3.9nH, Eq. (1). This capacitor selection value proved to be interesting, as discussed later. If we used the correct value of ESL, the self-resonant frequency along with other details provided in Table 1 now makes sense. Trace inductance of a microstrip transmission line on this PCB stack is 7-nH/cm (18-nH/inch).

$$f = \frac{1}{2\pi\sqrt{ESL * C}} \tag{1}$$

Radiated emission, E (μV/m) from the loop area between capacitor and component can be easily determined by Eq. (2) [7]. Current draw is 380 mA under maximum load conditions. The variables in (2) involve f = frequency in MHz, A=loop area (m), I_{dm} = current (mA), and r = distance between PCB and antenna (meters). Three meters is used to represent FCC Class B limits.

$$E = 263\times10^{-16}(f * A * Idm)\left(\frac{1}{r}\right) \tag{2}$$

Equation (3) calculates the wavelength of a propagating signal and is related to total loop perimeter from capacitor placement, with f = frequency (MHz) and λ = wavelength (meters). This is the frequency in which the loop area becomes an efficient antenna. Consequently, any loop size from decoupling capacitor placement being very small, cannot become an efficient radiating differential-mode or loop antenna. Test data and plots confirmed this.

$$f = \frac{300}{\lambda} \tag{3}$$

The physical location of a decoupling capacitor, if routed with a trace to a component, allows a loop to exist. This loop does have an effect on radiated emissions, but not based on the actual physical size of the loop.

Amplitude levels from all decoupling locations were nearly identical when measured in a TEM cell, indicating size of the loop *did not* have significant effect on radiated EMI.

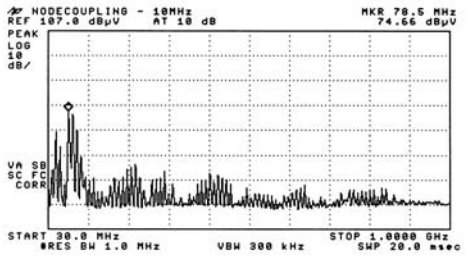
Radiated emission from the PCB with different decoupling capacitor values is provided in Fig. 3. Regardless of decoupling loop size, radiated emissions were exactly identical which indicates that the size of a decoupling loop makes no difference in EMI, since EMI is being radiated with significant magnitude from somewhere else and not from the loop or its physical size.

One reason why a decoupling loop may cause radiated EMI is explained by [6], which had a piece of wire attached to a plane driven by common-mode currents present within the PDN. Ref. [6] did not investigate traces routed microstrip, the focus of this paper. When a transmission line (trace) is energized with common-mode current created as a result of insufficient decoupling or interplane capacitance, common-mode currents developed internal to the component now have an antenna to propagate EMI from.

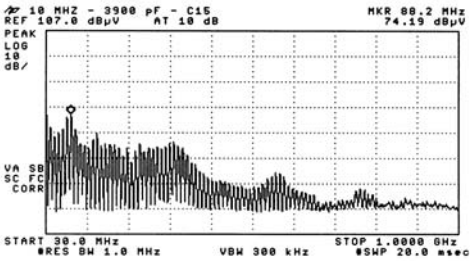
Table 1. Parametric Details of the Test PCB

Capacitor ID	Loop perimeter due to capacitor placement	Total loop inductance [1]	Self-resonant frequency of the loop path[3]	Calculated emission levels @ 10 MHz[4]	Calculated radiated frequency (loop area)[5]
C11	2.5 inches (6.4 cm)	46 nH	11.5 MHz	108.8 μV/m	4.8 GHz
C12	3.0 inches (7.6 cm)	55 nH	10.8 MHz	153.4 μV/m	3.9 GHz
C13	3.5 inches (8.9 cm)	64 nH	10.0 MHz	210.3 μV/m	3.4 GHz
C14	4.0 inches (10.2 cm)	73 nH	9.4 MHz	276.3 μV/m	2.9 GHz
C15	4.5 inches (11.4 cm)	82 nH	8.9 MHz	345.1 μV/m	2.6 GHz
C16	0.01 inches (0.25 mm)	3.18 nH [2]	45.2 MHz	0.17 μV/m	1,200 GHz

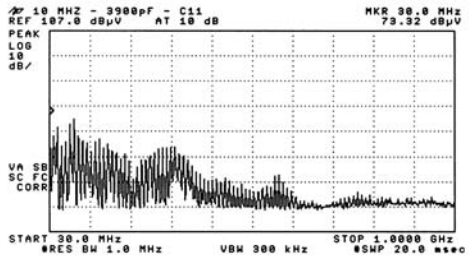
1. Includes package lead-length inductance (1-nH) and trace inductance from the total loop area (18 nH/inch).
2. Inductance value contains lead-length inductance (1-nH) and one via (2-nH).
3. Value of capacitor used for calculating self-resonant frequency, Eq. (1): 3900 pf (3.9 nF) and total loop inductance, *L*.
4. Distance used is 3 meters, calculated from Eq. (2).
5. Loop area determined from loop perimeter for use with Eq. (3).



No decoupling capacitor – 10 MHz



Worst case decoupling, 3.9 nF–11.4cm (4.5"), 10 MHz



Typical decoupling location, 3.9 nF–6.4cm (2.5") 10 MHz

Figure 3. Radiated emissions from sample loop areas.

A dipole antenna is created by the existence of the decoupling loop, with the driven element at voltage potential and the ground element at 0V. When any capacitive element is installed between the two elements of a dipole antenna, common-mode current propagates through the capacitor which closes the RF loop for AC currents. The capacitor's dielectric emulates free space conditions, allowing common-mode current developed internal to a component to drive this virtual dipole antenna if plane bounce occurs. This concept is illustrated in Fig. 4 [3, 4].

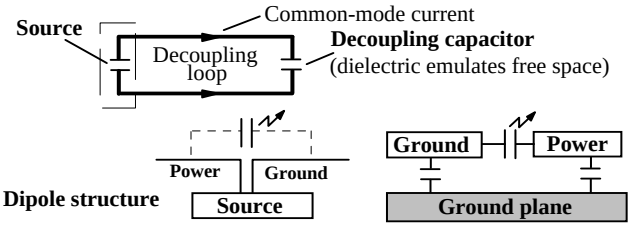


Fig. 4. Antenna structure due to decoupling placement

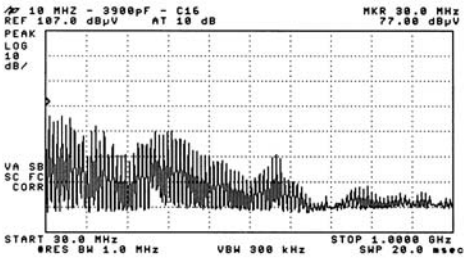
The loop area on PCBs between a capacitor and component is physically small, which means they become an efficient radiating loop antenna in the GHz range. Decoupling capacitors do not provide decoupling in this frequency range. Decoupling capacitors instead creates a dipole antenna structure but only if there is a routed trace and not via directly to a PDN. We must concern ourselves with common-mode current developed from driving a dipole antenna.

The self-resonant frequency of a 3.9 nF, surface mount capacitor (0805 package size) with lead length inductance of 1-nH is 80 MHz, as long as the capacitor *is never installed* on the PCB. When installed on the PCB, lead inductance reduces the self-resonant frequency from 80 MHz to approximately 10 MHz. Investigation occurred at both 80 MHz and 10 MHz.

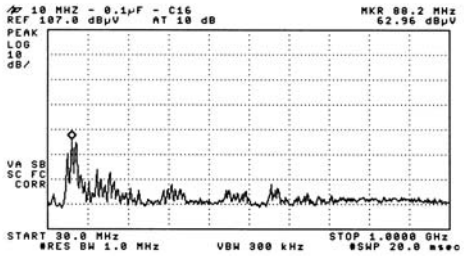
Radiated emissions were measured with different capacitance value to determine differences in radiated emissions from the size of the loop. Fig. 4 shows replacing the 3.9 nF capacitor (chosen because it was supposed to be self-resonant at 80 MHz) with a 100 nF capacitor. The 100 nF capacitor is self-resonant at 16 MHz, using actual trace inductance. The 3.9 nF capacitor, located in a best-case physical position (C16), is resonant at 45 MHz. The 3.9 nF capacitor is self-resonant at approximately 10 MHz at locations C11-C15.

If physical placement has no effect on emissions, then why was less radiated EMI observed with the 100 nF capacitor? This was the result of having a *greater amount of stored electrical charge* provided by the larger value capacitor, not loop area dimension. The 3.9 nF capacitor, with limited energy storage operating at 45 MHz, could not provide sufficient energy to the component operating at both 10 MHz and 80 MHz. Figure 5 illustrates effects of five identical value decoupling capacitors in parallel to increasing charge storage. The net effect is that the total amount of energy to the 74FCT244 is five times greater. The greater the charge energy at the operating frequency of the device, a reduction in radiated emission is observed. Reduced EMI occurs

because the component produces less common-mode current since the PDN is now providing sufficient charge to keep the planes from bouncing due to lack of energy storage.



Minimum loop dimension possible, 3.9 nF – 10 MHz



Minimum loop dimension possible, 0.1 µF - 10 MHz

Fig. 4. Effect of different capacitor values, same location

III. CONCLUSION

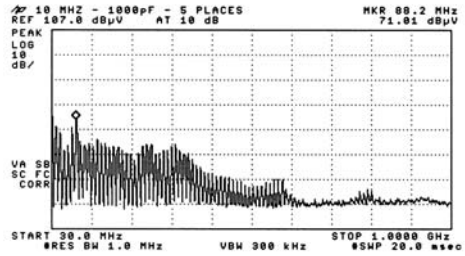
The dimension of a decoupling loop, due to capacitor placement, does play a role in amplitude development and propagation of RF emissions. The perimeter of the loop emulates a dipole antenna, radiating common-mode energy, with the magnitude of EMI identical regardless of loop size. The capacitor acts as the driven portion of the antenna structure due to an imbalance in the differential-mode power distribution network if both power and return traces are not exactly identical in length. A very small loop does not generate any greater magnitude of radiated emissions than a capacitor located further away with a larger loop size although spectral shifts are observed. This situation is valid as long as any trace exists on either the top or bottom of the PCB, but does not apply if the capacitor is connected directly to planes by vias to minimize lead inductance.

If sufficient amount of charge storage is provided, the silicon internal to a component package will not bounce planes to any degree. When planes bounce occurs common-mode current is developed which now sees a dipole structure to drive the trace. To prevent this situation from occurring, never use a routed trace between component and decoupling capacitor.

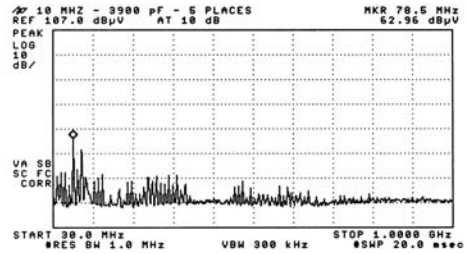
If EMI occurs that cannot be easily identified from where the energy is coming from, and if there is a decoupling capacitor with a routed trace, remove this capacitor. There is probably sufficient amount of decoupling already present and removing one capacitor may not cause functional disruption.

REFERENCES

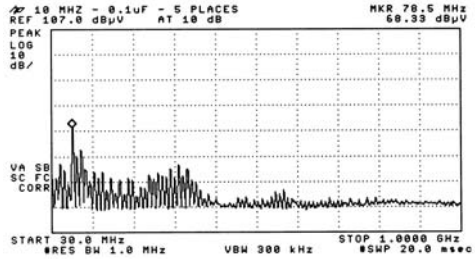
1. Drewniak, J. L., T. H. Hubing, T. P. Van Doren, D. M. Hockanson. "Power Bus Decoupling on Multilayer Printed Circuit Boards." *IEEE Transactions on Electromagnetic Compatibility* 37(2), 1995. 155-166.



Five capacitor – 1 nF (5 nF total) – 10 MHz



Five capacitor – 3.9 nF (20 nF total) – 10 MHz



Five capacitor – 100 nF (500 nF total) – 10 MHz

Fig. 5. Magnitude of emissions - multiple capacitors

2. T. P. Van Doren, J. Drewniak, T. H. Hubing. "Printed Circuit Board Response to the Addition of Decoupling Capacitors," Tech. Rep. #TR92-4-007, University of Missouri, Rolla EMC Lab., 1992. (September 30).
3. Montrose, M.I. Analysis on Loop Area Trace Radiated Emissions from Decoupling Capacitor Placement on Printed Circuit Boards. *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 1999. 423-428.
4. Montrose, M.I. 2000. *Printed Circuit Board Design Techniques for EMC Compliance*. Wiley/IEEE Press.
5. Paul, C.R. "A comparison of the contributions of common-mode and differential-mode currents in radiated emissions." *IEEE Transactions on Electromagnetic Compatibility* 31, 2:189-193.
6. Drewniak, J. L., T. H. Hubing, T. P. Van Doren. 1994. "Investigation of Fundamental Mechanisms of Common-Mode Radiation from Printed Circuit Boards with Attached Cables." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 1989. 110-115.
7. Ott, H. 1988. *Noise Reduction Techniques in Electronic Systems*, 2nd ed. New York: John Wiley & Sons, Inc.
8. Tang, G. "Surface Mount Capacitor Loop Inductance Calculation and Minimization." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 1998. 505-510.
9. Yuan, F. "Analysis of Power/Ground Noises and Decoupling Capacitors in Printed Circuit Board Systems." *Proceedings of the IEEE International Symposium on Electromagnetic Compatibility*, 1997. 425-430.