Component Performance Associated with Power/Return Plane Bounce Using Board Edge Termination

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Abstract–This paper illustrates effects on digital components due to reflected EM waves created by different board edge termination methodologies. Depending on the physical location of a digital device, relative to the edge of the printed circuit board (PCB), either a voltage or return plane bounce may occur that exceeds operational margin levels of these devices

Regardless of design techniques implemented or simulation analysis performed, undesired RF field development will still occur within any power distribution network (PDN), which for most electrical products, is both a power and a return plane (0V reference or ground).

Common-mode currents within a PDN are developed by large repetitive impulse currents demanded by digital circuits. This is caused by inadequate decoupling that serves as charge storage, along with board resonances. With a non-optimized PDN, simultaneously switching noise (SSN) as well as electromagnetic interference may occur. In addition, if the bounce on either the voltage and/or return plane exceeds voltage reference levels, devices may not function reliably.

Index Terms— 20-H Rule, board edge radiated emissions, ground bounce, printed circuit board (PCB), power bounce, RC plane termination, SSN, signal integrity.

I. INTRODUCTION

Common-mode radiated EMI is created by digital components switching logic states and transferring data through transmission lines, commonly called traces. In order to achieve this goal, all active devices must be connected to a PDN, namely power and return. Whether power and return are from traces or planes, the available power to the silicon die may exceed the current carrying capabilities of the PDN for a finite time period. Both signal integrity (SI) and electromagnetic interference (EMI) is created from the effects of a poor PDN.

Regardless how well we design the PDN, simultaneous switching noise (SSN) will be present. Our concern is the magnitude of the SSN observed by active components when voltage levels exceed operational parameters. When switching noise is present, it manifests itself into what is commonly called ground bounce. In reality, there is no such thing as ground bounce since a true ground does not exist within electrical products. We have power and return therefore, proper terminology is return bounce. The problem when one focuses only on return bounce is that power is also sourcing current at the same time return is sinking, generally at values that far exceed those observed only on return. When analyzing power and return plane bounce, this is generally performed in the time domain with simulation software or an oscilloscope. However, common-mode emissions, which can be significant, are easily measured with a spectrum analyzer.

This paper investigates the effects of plane bounce to digital components when a poor PDN is provided, and if active components will continue to function properly when the magnitude of either power or return bounce exceed operational values.

II. OVERVIEW ON PDN STRUCTURES

Power and return planes must be analyzed as transmission lines. Planes are no different in functionality than signal traces [1, 2, 3]. Planes that comprise a PDF must be terminated in their characteristic impedance. If improper or lack of termination exist at the physical edges of the PCB, a propagating wave will be reflected back to somewhere within the PCB structure. The voltage magnitude of the reflected wave and percentage of the reflection is easily calculated by (1) and (2), respectively.

$$V_r = V_o\left(\frac{Z_{Load} - Z_o}{Z_{Load} + Z_o}\right) \tag{1}$$

$$\%\,reflection = \left(\frac{Z_L - Z_o}{Z_L + Z_o}\right) \times 100 \tag{2}$$

where:
V_r = Reflected voltage level (V)
Vo = Output voltage of the driver (V)
Z_{Load} = Impedance of the PCB edge (Ω)
Z_o = Impedance of the transmission line (Ω)

The magnitude of plane bounce, V_b, (3) is determined by the total amount of current consumed over a finite time period along with total interconnect inductance.

$$V_{power/return} = L_{power/return} \frac{dI_{consumed}}{dt} \quad (3)$$

where:
V = bounce level on power or return system (V)
L = total interconnect inductance (H)
dI = total current consumption (A)
dt = actual switching time (sec.)

Within every PCB there are numerous reflected waves, one created from each power and return pin. This could result in dozens to thousands of propagating fields present at the same time. The magnitude of PDN bounce is usually minimal at device locations where a significant amount of charge storage is available. We should be concerned when improper or lack of charge storage (e.g., use of decoupling capacitors) exists in addition to when the PDN has high impedance at a particular x-/y-axis location.

With multiple outgoing and reflected waves present at a particular point of time, phase addition or subtraction may occur. If the magnitude of phasing, along with ringing amplitude is minimal, typical of most PDN networks, the RF propagating field present may appear to be at DC levels.

With phase addition of multiple reflected waves, if the magnitude of ringing exceeds voltage threshold levels, functional problems may occur if edge termination is not present.

Board edge radiated emissions analyzed as a transmission line is presented in [2], which examined external radiated field effects. Herein we use the identical configuration except with different observation points to observe propagated fields that traverse *back into the center of the PCB*.

III. TEST CONFIGURATION AND MODEL

Three primary means for terminating a PDN exist; via stitching [4], use of discrete RC components (impossible to implement but simulated herein), and the 20-H Rule (x-H). We use both the x-H Rule (where x-represents the recessed distance of the power plane from the board edge based on plane separation "*H*", and which is a number that can vary based upon application [3]) and RC termination to ascertain if reflected waves from the physical edge of the board will create excessive voltage fluctuations in the PDN, potentially causing SSN and EMI.

We utilized multiple stimuli simultaneously at different frequencies using HFSS, a Finite Element Method simulation program by Ansoft Corp.

The test configuration is illustrated in Fig. 1. Physical location of the three stimulus sources is identified as *S1*, *S2* and *S3*. Small solid rectangles denote five observation points (Obv.) - P(x). Figure 2 illustrates the simulation model for HFSS. A shield plane is required above the power plane; to prevent z-axis EMI as discussed in [2].

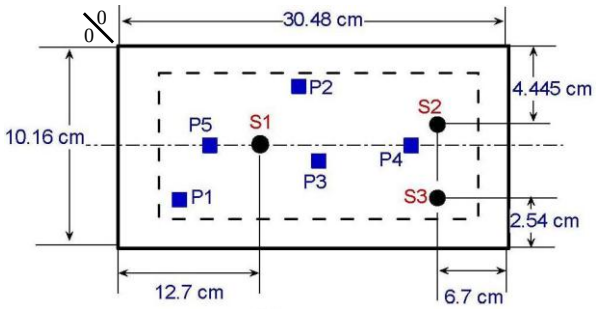


Fig. 1. PCB configuration (source/load locations)

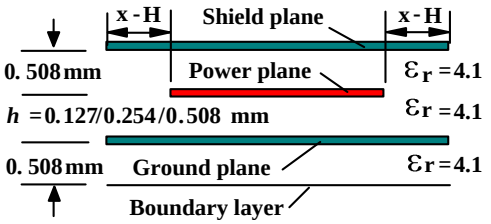


Fig. 2. Simulation configuration for HFSS

The five observation points [P(x)] represent where digital components may be physically located. These devices could be subjected to SSN within the PDN from reflected waves returning from the board edge and are listed in Table 1.

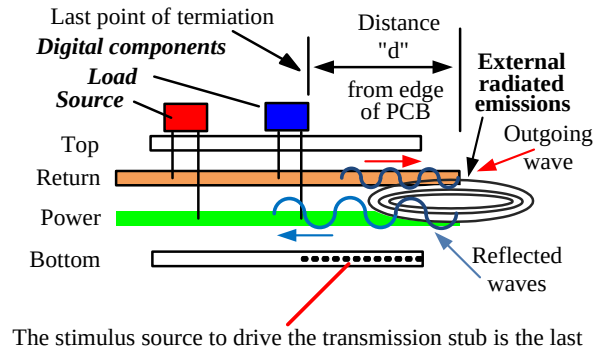
Table 1. Location of observation points

Port #	X Coordinate (cm)	Y Coordinate (cm)
P1	8.5	2.0
P2	2.5	14.0
P3	6.0	15.24
P4	5.08	20.0
P5	5.08	6.7

Depending upon the physical distance between a component and the edge of the assembly, additive phasing of multiple reflected waves may occur, whose bounce level cause by the ringing which occurs during reflective wave switching, may exceed operational margins of active components.

Test parameters for simulation:
Distance spacing between power/return planes (h):
0.127 / 0.254 / 0.508 mm (5/10/20 mils)
Stimulus: 300/600/900 MHz and 1.2/1.5 GHz
Stimulation: 1-amp current source between the planes
Source and observation locations: See Fig. 1.

In Figure 3, we have both external and internal reflected waves based on the physical location where components are located relative to the board edge.



The stimulus source to drive the transmission stub is the last components on the net. Distance "d" to the physical edge represented an un-terminated stub between component and edge of board (phase added reflections from multiple stimuli)

Fig. 3. Reflected wave propagation within a PDN

IV. IMPEDANCE ANALYSIS OF THE PDN

Figure 4 and Table 2 details PDN impedance (|Z|) based on numerical simulation. The further apart the planes are physically separated, the higher the impedance value [2].

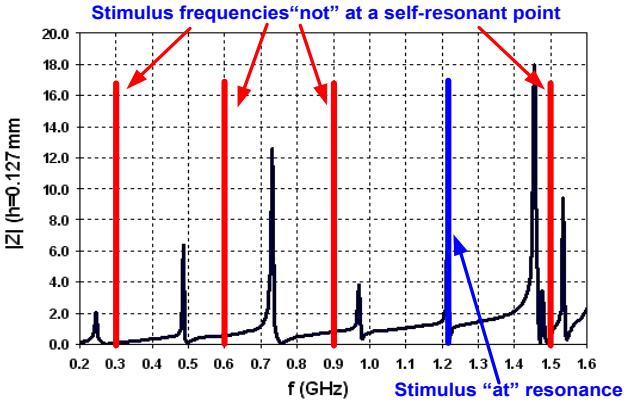


Fig. 4. Resonant frequencies of the PCB model

Table 2. Impedance of the PDN, different configurations

Frequency	Distance spacing between planes		
	h=0.127 mm	*h=0.254 mm*	*h=0.508 mm*
0.3 GHz	0.13 ohms	0.25 ohms	0.50 ohms
0.6 GHz	0.59 ohms	1.19 ohms	2.38 ohms
0.9 GHz	0.79 ohms	1.59 ohms	3.18 ohms
1.5 GHz	0.61 ohms	1.22 ohms	2.45 ohms

V. ANALYSIS: X-H RULE TERMINATION

Three different power and return plane distance separation distances using the x-H Rule with three simultaneous stimulus at the same frequency (*S1-S3*) is analyzed. By examining a large matrix of data, effects from phasing of multiple reflected waves from the board edge back into the center of the PCB, where digital components might be located, is determined.

Tables 3, 4 and 5 are simulation results where the value given is the amount of plane bounce at that specific location. Figure 5 provides visualization of this simulation results using a histogram.

The magnitude of plane bounce at certain locations and with different stimulus frequencies easily exceeds operational margins of components, *but only if plane resonance is high at that specific x-/y-axis location*, in addition to plane spacing distance and implementation of the x-H rule.

Common-mode currents due to plane bounce is observed as SSN and EMI, developed from the silicon die if noise voltage margins exceed operational parameters in consonant with distance separation between planes. For some configurations, as much as several volts of bounce will be present! Voltage levels above 1 Volt are highlighted in Tables 3-5 in bold face, and are more prevalent when distance spacing between the planes is greater that 0.127mm (5 mils).

VI. ANALYSIS: RC TERMINATION

To determine if x-H Rule termination provides enhanced power bus noise reduction, an RC network (R=2 ohms, C=20 pF) was substituted at the physical edge. The y-axis had nine (9) RC pairs and x-axis had four (4) or a total of 26 terminations. To ensure accurate, comparative analysis, simulation parameters were identical. Results are in Tables 6, 7 and 8.

Data indicates the RC termination network to minimize planar bounce is superior to x-H for certain PCB physical configurations. The observation points where x-H *performs better* is highlighted in bold face, which was infrequent. At 1.2 GHZ, *a significant amount of noise voltage was present due to the high plane impedance at this frequency which was simulated to observe effects of stimuating a PCB at both resonant and non-resonant frequencies.*

[Note-Bold face values in Tables 6-8 show that the x-H Rule is superior to RC].

VII. ANALYSIS: THREE DIFFERENT FREQUENCIES SIMULTANEOUSLY

To analyze effects of PCB edge termination to minimize reflected waves traveling back into the center of the PCB, three different frequencies were stimulated simultaneously to observe phasing effects at all five observation points. Table 9 details results. Due to extreme similarity between configurations, only the distance spacing of 0.127 mm is provided. Voltage levels greater than 0.5V are highlighted in bold face to illustrate effects of the PCB's inherent self-resonant frequency associated to the creation of plane bounce which may cause circuits to malfunction due to excessive SSN.

Table 3. Maximum bounce voltage with ***h*=0.127 mm**
Bold face indicates possible component failure

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-10h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P1-20h	0.24 V	0.10 V	0.44 V	0.62 V	**4.71 V**
P2-0h	0.10 V	0.23 V	0.34 V	**2.59 V**	0.41 V
P2-10h	0.10 V	0.22 V	0.50 V	**2.11 V**	0.43 V
P2-20h	0.10 V	0.22 V	0.35 V	**1.59 V**	0.80 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-10h	0.15 V	0.18 V	0.22 V	0.24 V	**1.60 V**
P3-20h	0.16 V	0.18 V	0.56 V	0.09 V	0.16 V
P4-0h	0.38 V	0.17 V	0.10 V	**1.91 V**	0.47 V
P4-10h	0.17 V	0.01V	0.18 V	**2.30 V**	**7.14 V**
P4-20h	0.41 V	0.19 V	0.12 V	**1.25V**	**2.11 V**
P5-0h	0.16 V	0.01V	0.19 V	**2.72 V**	0.45 V
P5-10h	0.17 V	0.01 V	0.18 V	**2.30 V**	**7.14 V**
P5-20h	0.19 V	0.01 V	0.15 V	**1.76 V**	0.40 V

Table 4. Maximum bounce voltage with ***h*=0.254 mm**
Bold face indicates possible component failure

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.47 V	0.21 V	0.49 V	**0.97 V**	0.49 V
P1-10h	0.53 V	0.20 V	**1.24 V**	**1.06 V**	0.84 V
P1-20h	0.63 V	0.19 V	0.32 V	0.88 V	**9.45 V**
P2-0h	0.19 V	0.46 V	0.67 V	**4.69 V**	0.81 V
P2-10h	0.20 V	0.45 V	0.81 V	**3.21 V**	**1.43 V**
P2-20h	0.20 V	0.43 V	0.12 V	**2.49 V**	**10.0 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	**1.19 V**
P3-10h	0.31 V	0.36 V	**1.17 V**	0.09 V	0.61 V
P3-20h	0.33 V	0.38 V	0.74 V	0.31 V	**13.7 V**
P4-0h	0.75 V	0.34 V	0.21 V	**3.48 V**	0.75 V
P4-10h	0.81 V	0.37 V	0.23 V	**2.57 V**	**3.94 V**
P4-20h	0.89 V	0.40 V	0.23 V	**2.08 V**	**13.3 V**
P5-0h	0.32 V	0.02 V	0.38 V	**4.96 V**	**1.03 V**
P5-10h	0.37 V	0.01 V	0.32 V	**3.64 V**	**1.04 V**
P5-20h	0.44 V	0.01 V	0.26 V	**2.89 V**	**9.39 V**

Table 5. Maximum bounce voltage with ***h*=0.058 mm**
Bold face indicates possible component failure

Obv. Pt.	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.97 V	0.42 V	**1.21 V**	**1.68 V**	0.64 V
P1-10h	**1.17 V**	0.39 V	0.21 V	**1.76 V**	**33.8 V**
P1-20h	**1.63 V**	0.36 V	**121.5V**	0.65 V	0.19 V
P2-0h	0.38 V	0.92 V	**1.52 V**	**8.38 V**	**1.97 V**
P2-10h	0.40 V	0.88 V	0.52 V	**5.41 V**	**41.9 V**
P2-20h	0.40 V	0.86 V	**106.8V**	**3.26 V**	**2.08 V**
P3-0h	0.58 V	0.70 V	**1.06 V**	0.38 V	**3.63 V**
P3-10h	0.64 V	0.74 V	**1.38 V**	0.39 V	**61.8 V**
P3-20h	0.73 V	0.78 V	**45.51V**	0.45 V	0.11 V
P4-0h	**1.52 V**	0.69 V	0.44 V	**6.26 V**	**1.29 V**
P4-10h	**1.70 V**	0.76 V	0.47 V	**4.47 V**	**61.5V**
P4-20h	**2.07 V**	0.87 V	**3.74 V**	**3.82 V**	**1.24 V**
P5-0h	0.68 V	0.04 V	0.73 V	**9.02 V**	**1.99 V**
P5-10h	0.82 V	0.02 V	0.56 V	**6.20 V**	**41.5 V**
P5-20h	**1.20 V**	0.01 V	2.09 V	**5.22 V**	0.57 V

Table 6. Maximum bounce voltage with ***h*=0.127 mm** and (24) RC termination (R=2 ohms, C=20 pF).
Bold face indicates x-H Rule is better than RC

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.23 V	0.10 V	0.26 V	0.55 V	0.24 V
P1-0hRC	0.09 V	0.04 V	0.16 V	0.19 V	0.09 V
P2-0h	0.10 V	0.23 V	0.34 V	2.59 V	0.41 V
P2-0hRC	0.08 V	**0.26 V**	0.31 V	0.38 V	0.27 V
P3-0h	0.15 V	0.18 V	0.30 V	0.20 V	0.62 V
P3-0hRC	0.11 V	0.13 V	**0.41 V**	**0.26 V**	0.35 V
P4-0h	0.38 V	0.17 V	0.10 V	1.90 V	0.47 V
P4-0hRC	0.26 V	0.10 V	**0.21 V**	0.09 V	0.36 V
P5-0h	0.16 V	0.01 V	0.19 V	2.72 V	0.45 V
P5-0hRC	0.06 V	**0.04 V**	**0.38 V**	0.34 V	0.11 V

Table 7. Maximum bounce voltage with ***h*=0.254 mm** and (24) RC termination (R=2 ohms, C=20 pF).
Bold face indicates x-H Rule is better than RC

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.47 V	0.21 V	0.49 V	0.97 V	0.49 V
P1-0hRC	0.06 V	0.10 V	0.10 V	0.28 V	0.30 V
P2-0h	0.19 V	0.46 V	0.67 V	4.69 V	0.81 V
P2-0hRC	0.12 V	0.27 V	0.10 V	0.44 V	**1.15 V**
P3-0h	0.29 V	0.35 V	0.60 V	0.40 V	1.19 V
P3-0hRC	0.15 V	0.32 V	0.05 V	0.07 V	0.92 V
P4-0h	0.75 V	0.34 V	0.21 V	3.48 V	0.75 V
P4-0hRC	0.38 V	**0.35 V**	**0.40 V**	0.81 V	**0.79 V**
P5-0h	0.32 V	0.02 V	0.38 V	4.96 V	1.03 V
P5-0hRC	0.03 V	**0.12 V**	0.22 V	0.70 V	0.51 V

Table 8. Maximum bounce voltage with ***h*=0.508 mm** and (24) RC termination (R=2 ohms, C=20 pF).
Bold face indicates x-H Rule is better than RC

Obv. Point	300 MHz	600 MHz	900 MHz	1.20 GHz	1.50 GHz
P1-0h	0.97 V	0.42 V	1.21 V	1.68 V	0.64 V
P1-0hRC	0.26 V	0.02 V	0.06 V	1.03 V	**2.10 V**
P2-0h	0.38 V	0.92 V	1.52 V	8.38 V	1.97 V
P2-0hRC	0.13 V	0.10 V	0.53 V	0.57 V	**3.66 V**
P3-0h	0.58 V	0.70 V	1.06 V	0.38 V	3.63 V
P3-0hRC	0.15 V	0.23 V	**1.08 V**	**0.96 V**	1.71 V
P4-0h	1.52 V	0.69 V	0.44 V	6.26 V	1.29 V
P4-0hRC	0.37 V	0.47 V	**1.89 V**	0.99 V	**1.96 V**
P5-0h	0.68 V	0.04 V	0.73 V	9.02 V	1.99 V
P5-0hRC	0.09 V	**0.10 V**	0.27 V	1.06 V	**2.58 V**

VIII. VALIDATION OF SIMULATION MODEL

To validate our simulation model, the cavity model detailed in [6] is compared against our HFSS model. The solid line is our simulated results where validation is identified by triangles which show nearly perfect correlation. Validation is thus confirmed. Using the superposition principal is also valid for components located anywhere within the PCB.

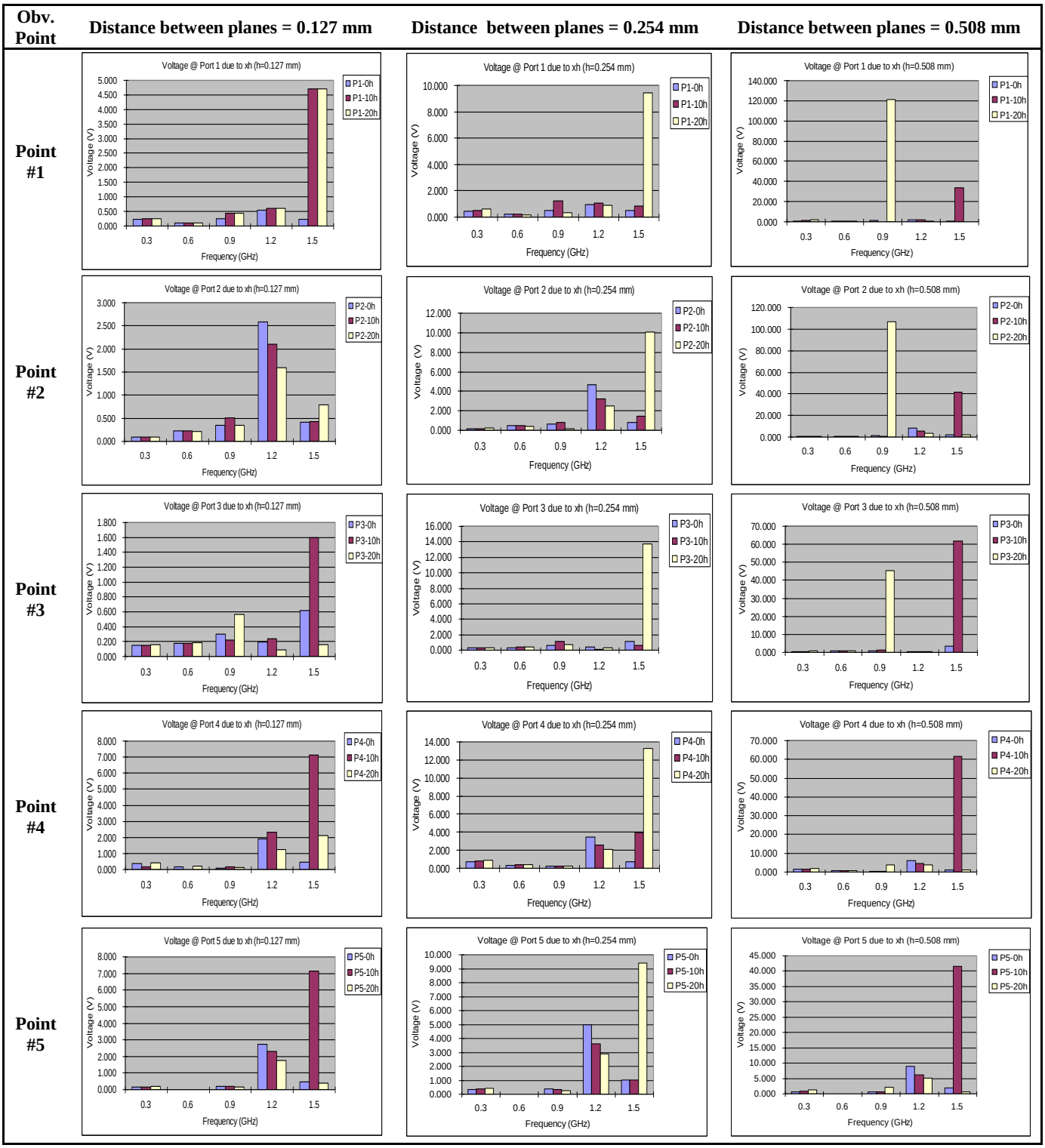


Fig. 5. Planar bounce using x-H Rule termination
Large values indicate possible system failure to digital components due to excessive SSN or plane bounce

A 1A current source was provided at each stimulus port per previous analysis. To validate our data as accurate, we now choose only one current source at Port *S1* with the observation point Port *P3*. A rectangular air box enclosing the PCB is used to implement the radiation boundary condition required for simulation. Results from validation are provided in Fig. 6.

Table 9. Maximum voltage bounce with three different stimulus sources simultaneously, ***h=0.127 mm***

Obv. Point	S1 (0.3GHz) S2 (0.6GHz) S3 (0.9GHz)	S1 (0.6GHz) S2 (0.9GHz) S3 (1.5GHz)
P1-0h	0.49 V	0.31 V
P1-10h	**0.62 V**	0.39 V
P1-20h	**0.63 V**	0.14 V
P2-0h	0.25 V	0.44 V
P2-10h	0.36 V	0.48 V
P2-20h	0.37 V	0.39 V
P3-0h	0.21 V	**0.50 V**
P3-10h	0.14V	**0.53 V**
P3-20h	0.40 V	**0.82 V**
P4-0h	0.08 V	0.44 V
P4-10h	0.08 V	0.46 V
P4-20h	**0.87 V**	0.62 V
P5-0h	0.34 V	0.27 V
P5-10h	0.34 V	0.26 V
P5-20h	0.33 V	0.42 V

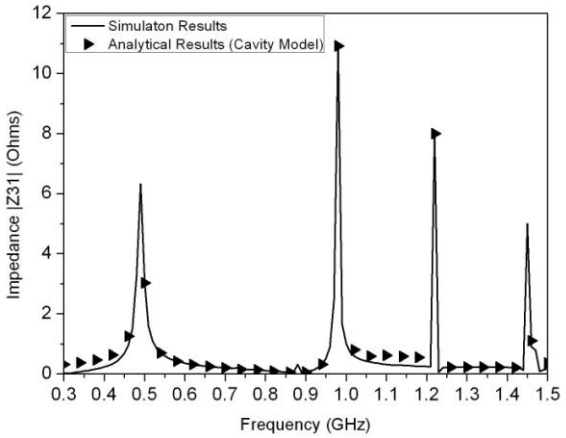


Fig. 6. Validation of simulation results

IX. COMMENTS ON TEST DATA ANOMALIES

Several voltage bounce (SSN) values in Tables 3 through 9 are extremely high, or unrealistic. With complex impedance present within the PDN scattered throughout the assembly, and the inabillity to simulate every conceivable source load location, one may never know if a problem exist when using a simple model. It is impossible to physically probe all source or load locations on a PCB if one does not know what to look for and where.

To explain why a large voltage value, or bounce occurs using a simple example, we excite the plane pair at *S1* using current *I1*, with a voltage response *V3* at *P3* per Eq. (1).

$$Z_{31} = \frac{V_3}{I_1} \text{ (ohms)} \qquad (1)$$

From Fig. 6, at 0.98 GHz, the |*Z31*| impedance is approximately 11 ohms. Exciting *S1* with a 1A current source, the voltage response (magnitude) at *P3* will thus be 11 volts. This volt exists because the impedance between the planes consists of a complex number. We can easily convert the y-axis of Table 6 to $V_{magnitude}$, which is how the data in Tables 3 through 9 is presented. If impedance at any location in the PDN is high, a large bounce condition will exist.

When multiple reflecting waves adding in phase, and a high magnitude at a resonant frequency of the PDN is present, along with a complex impedance, anomalies may occur as high levels of SSN. All data herein illustrates a *theoretical situation*. This does not mean excessive plane bounce will exist in a real PCB. There are numerous losses within the PCB material and dielectric to prevent this problem from occurring. Also, there are generally an undetermined number of reflected waves bouncing around from the edge to middle of the PCB due to many components switching logic states simultaneously. Phasing of many signals at the same time generally result in little SSN and is generally broadband.

When using simulation exclusively to analyze a PCB, sometimes results may seem unreasonable but are acceptable if they can be explained using physics and mathematics, or Ohm's law. An unexpected problem may never be discovered if only a single souce stimulus and one load is investigated. Performing extensive simulations with many variables help us understand potential problems.

In reality, every PCB mandates use of decoupling capacitors. Discrete capacitors pull the impedance of the PDN to a very small value, usually in the order of 1 ohm or less, but *only* within a limited bandwidth of operation of the discrete device. The item of concern, and which is presented herein, is a concept that must be understood by designers, that a SSN problem *may occur if the impedance of the board is high at a particular physical location, which is not lowered by use of discrete decoupling capacitors or a buried capacitive structure*.

It can thus be implied that use of decoupling capacitors in sections of the PCB (unpopulated areas) without any components may be required to lower PDN impedance and prevent reflected waves from causing system level problems.

X. CONCLUSION

Real-world printed circuit boards have numerous stimulation sources, namely the power and return pins of digital component. Every time a component sources or sinks current from a power distribution network, plane bounce will occur. Power and return planes behave identical to signal transmission lines. There is no difference between terminating planes or signal

transmission lines. Un-terminated transmission lines allow signal integrity problems (SSN) as well as EMI to be developed. For plane termination there are several techniques available. Two different plane termination techniques were analyzed to determine if these techniques minimize SI and EMI; x-H Rule and RC.

When determining which board edge termination methodology performs best using simulation analysis, results will differ based on input parameters. These parameters include physical source location, observation points, distance spacing between planes, physical dimensions of the planes in the x-/y- axis, voltage/current amplitude of the stimulus source(s), the stub length of each transmission line from a component to the physical edge of the board, and other parameters not listed. A designer must anticipate all resonant frequencies and phasing effects of reflected wave propagation within a PDN before beginning full board-level simulation, and how each stimulus source reacts based upon multiple source frequencies, which may be beyond the simulation capabilities of the software. Extensive computing resources are required for comprehensive analysis.

A transmission line stub will always exists between the physical location of a component and the board edge. This stub is one of two elements that comprise of dipole antenna. This antenna is one element that causes signal integrity and EMI to be developed and propagated.

A real-world PCB requires plane termination. Regardless of the termination methodology used, if the impedance at a physical location is high due to insufficient decoupling or a poor PDN, functional problems may occur to digital components.

XI. REFERENCES

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