Printed Circuit Board Suppression Concepts for EMC Compliance

PART 1

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This two-part article presents fundamental EMC concepts related to implementing suppression techniques for EMC compliance into printed circuit boards (PCBs). Part 1 appears in this issue of ITEM. Part 2 will be published in ITEM Update, 1998. Together these related articles create one comprehensive document. Both articles present reasons why and how EMC exists within a PCB, along with various design and layout techniques that are easy to incorporate. These design and layout techniques represent a fundamental approach to RF suppression during layout and at the beginning of a design project to minimize EMC threats. Topics examined in the next article will include routing clock traces, impedance control, trace termination, and alternate suppression layout techniques.

Introduction

In today's international marketplace, products must conform to a host of regulations, standards and requirements mandated by government agencies, private standards organizations, and voluntary councils. Mandatory compliance requirements exist for North America, the European Union (EU), and numerous countries worldwide. These regulations cover EMC and essential requirements for product safety.

It is more cost-effective to use design and layout techniques for suppression of EMC within a printed circuit board (PCB) than to rely upon containment measures provided by a metallic enclosure. Top covers, filler panels, I/O adapter brackets, and the like can be removed or damaged by the end user. Sometimes, these items are not designed or manufactured correctly. A system must maintain compliance to EMC standards for as long as the unit provides an intrinsic function to a user. Containment cannot be relied upon for lifetime protection, whereas suppression is always there.

Three elements must be present for EMI to exist. These three elements are: noise source, propagation path, and susceptor. Noise source on a PCB relates to frequency-generating circuits, component radiation within a plastic package, ground bounce, electrically-long trace lengths, poor impedance control, cable interconnects, and the like. Propagation path refers to the medium that carries the RF energy, such as free space or a metallic interconnect. Susceptor is the device which receives undesired RF interference. If one of these three elements is removed, an EMI event cannot exist. It is our task to determine which of the three is the easiest to eliminate. We have no control over the susceptor, as we generally do not know what the susceptor will be. Suppression affects noise source, and is the easiest of the three to implement.

A product must be designed for two levels of performance: one to minimize RF energy leaving an enclosure (referred to as emissions), and the other to minimize the amount of RF energy entering the enclosure (to ensure immunity). When dealing with emissions, a general rule of thumb applies: *The higher the frequency, the greater the likelihood of a radiated coupling path; the lower the frequency, the greater the likelihood of a conducted coupling path.*

Five major considerations exist for EMC analysis, (referred to as "FATID" by Bill Kimmel and Daryl Gerke)[1]:

- *Frequency.* Where in the frequency spectrum is the problem observed?
- *Amplitude.* How strong is the source energy level, and how great is its potential to cause harmful interference?
- *Time.* Is the problem continuous (clock signals), or does it exist only during certain cycles of operation (e.g., disk drive write operation or network transmission)?
- *Impedance.* What is the impedance of the source and receptor along

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with the impedance of the transfer mechanism between the two?

- *Dimension*. For transmission of RF energy to occur, an antenna is needed. The physical dimensions that exist, based on trace length or slots within an enclosure determine which particular frequencies are most likely to be observed.

How does RF energy get created within a PCB? Maxwell's equations, derived from Ampere's Law, Faraday's Law, and Gauss's Law describe the relationship between electric and magnetic fields. These equations describe the field strength and current density within a closed loop environment, details of which are beyond the scope of this article.

To oversimplify Maxwell, we relate his four equations to Ohm's Law. The presentation that follows is a simplified approach that allows one to visualize Maxwell in terms that are easy to understand. Although not mathematically perfect, this approach is useful in presenting Maxwell to non-EMC engineers or those with minimal exposure to PCB suppression concepts and EMC theory.

Ohm's Law: $V = I \bullet R$

Maxwell Made Simple:

$$V_{RF} = I_{RF} \bullet Z$$

where

V = Voltage
I = Current
R = Resistance
Z = Impedance (R + jwx)
RF = Radio frequency energy

Comparing *Maxwell Made Simple* to *Ohm's Law*, when RF current exists in a transmission line (PCB trace), which has a fixed impedance value, an RF voltage will be created that is proportional to the RF current. Notice that in the electromagnetics model, R is replaced by Z, a complex number which contains two components: resistance (R, a real component) and reactance (a complex component). For this transmission line example, capacitance does not exist. Each and every trace has a finite impedance value. The inductance that exists within a transmission line (trace) is one of several parameters that allows RF energy to be created within a PCB. The bond wires that connect a silicon die to its mounting pad may also be sufficiently long to add lead length inductance to the trace and to cause EMC concerns. Traces routed on a PCB can be highly inductive, especially traces that are physically long in routed length.

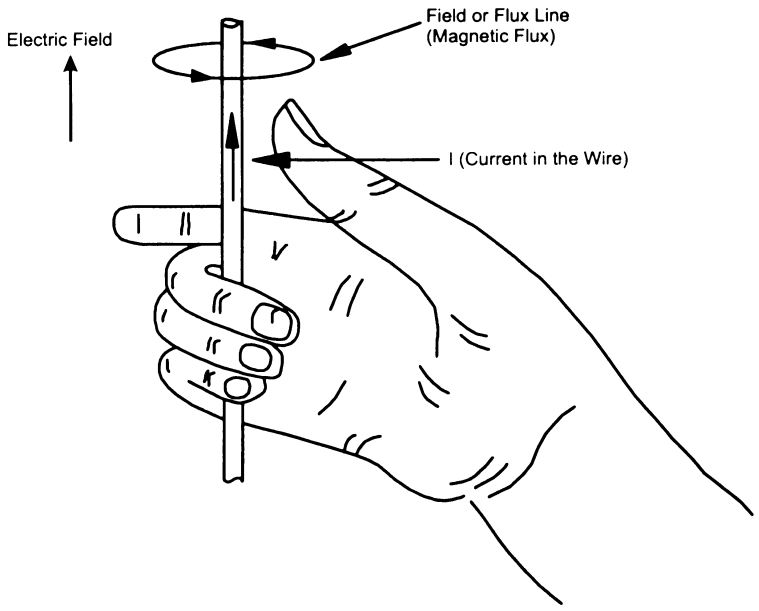

Figure 1. *Right Hand Rule.*

Returning to Maxwell, a moving electrical charge in a transmission line (trace) creates a magnetic field. Magnetic fields created by this moving electrical charge are identified as magnetic lines of flux. Magnetic lines of flux can easily be visualized using the Right Hand Rule (Figure 1). To observe this rule, make a loose fist with your right hand and point your thumb straight out. Current flow is in the direction of the thumb (upwards), simulating current flowing in a wire or PCB trace. Your curved fingers encircling the wire point in the direction the magnetic flux lines (field) travel. This magnetic flux creates a transverse electromagnetic field, commonly called the electric field. The mathematical relationship between magnetic and electric fields is beyond the scope of this article, however, readers should understand that RF emissions are a combination of both magnetic and electric field components. These fields will exit the PCB structure by either radiated or conductive means.

Note that a magnetic field must travel around a closed loop boundary. In a PCB, RF currents are created by a source driver and transferred to a load through a transmission line. RF currents must return to their source through a 0-V reference return system. As a result, a current loop is developed. This loop does not have to be circular, and is often a convoluted shape. Since we must have a closed loop circuit for operation, a source to load and its return path, a magnetic field is developed. This magnetic field creates a radiated electric field. Magnetic fields are typically observed with loop antennas in the near field ($\lambda/4$ of the frequency present), while electric fields are generally observed in the far field ($>\lambda/4$).

Another simplified explanation of how RF exists within a PCB is shown in Figure 2. Here we see a circuit diagram in both the time and frequency domains. A closed loop circuit must exist if the circuit is to work. When the switch is closed, the circuit is complete,

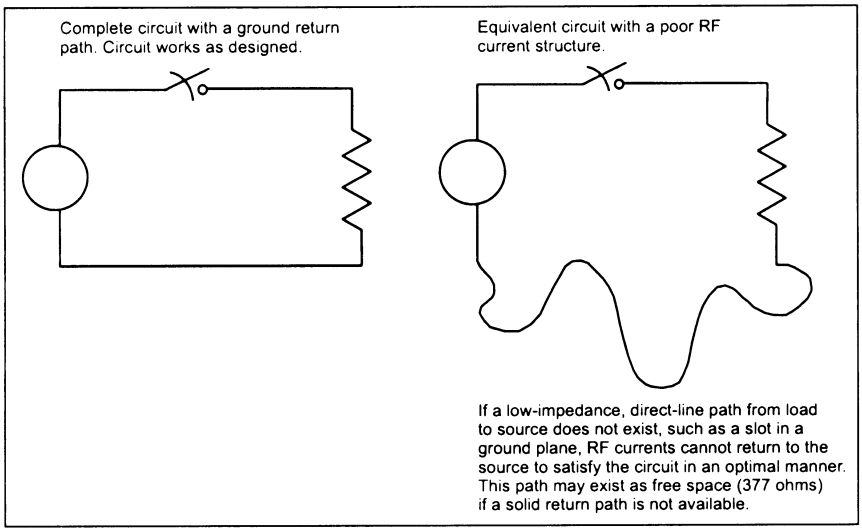

Figure 2. *Circuit Representation - Time and Frequency Domain.*

and AC or DC current flows (time domain). In the frequency domain, replace the time domain current (AC/DC) with RF current. The RF return path (frequency domain) from load to source must also exist or the circuit would not work. Hence, a PCB structure in both time and frequency domain must conform to Maxwell's equations, Kirchoff's and Ampere's law.

Return currents must travel through a 0-V reference structure (power supply return system), generally a ground trace or ground plane. When RF return current travels from load to source through a planar structure, this path is commonly called an image plane, reference plane or image return path. It is desirable to have the return path located as close as physically possible to the routed trace, discussed later. Because there is a finite, physical distance between the trace and the RF current return path, flux coupling between the magnetic field and the return structure will approach, but not quite reach 100%. *This finite amount of leftover RF current which is not coupled to a return structure is a primary cause of EMI within the PCB.*

Knowing one reason how RF energy is created within a PCB (generation of magnetic lines of flux from a trace), it becomes the designer's job to prevent this residual energy creation. The process of removing unwanted RF currents is called *flux cancellation.* In this author's opinion, flux cancellation is the most important design and layout requirement for RF suppression. The PCB must be designed for use in both the time and frequency domain. Regardless of how well a PCB is designed, both magnetic and electric fields will always exist. If magnetic flux is canceled, EMI cannot exist. It is that simple!

How do we *cancel the flux?* This is easier said than done. Recommendations for layout techniques include, but are not limited to:

- Assign proper stackup and impedance control for multilayer boards.
- Route clock traces adjacent to a 0-V reference plane (multilayer PCB) or use a ground or guard trace (single- and double-sided boards).
- Couple magnetic flux created internal to a component package into the 0-V reference system to reduce component radiation.
- Carefully choose logic families to minimize RF spectral distribution and trace radiation (use slower edge rate devices if possible).
- Reduce RF drive currents on traces by reducing the RF drive voltage from a clock generation circuit, e.g., TTL vs. CMOS drive levels.
- Reduce ground noise voltage within the power and ground plane structure.
- Provide sufficient decoupling for components when all device pins switch simultaneously under maximum capacitive load.
- Properly terminate clock and signal traces to prevent ringing, overshoot and undershoot (enhances signal quality).
- Use data line filters and common-mode chokes on selected nets.
- Properly use bypass (not decoupling) capacitors when external I/O cables and interconnects are provided.
- Provide a grounded heatsink for components that radiate large amounts of common-mode RF energy internal to the device package.

Image Planes and Stackup Assignments

Within a PCB, RF energy is created based on Maxwell's equations. Maxwell describes the existence of both electric charges and magnetic fields. In addition to Maxwell, Kirchoff's and Ampere's laws describe the operation of a circuit or network. Kirchoff's voltage law states that the algebraic sum of the voltage around any closed loop path in a circuit must be zero. Ampere's law describes the magnetic induction at a point due to given currents in terms of the current elements and their positions relative to that point.

If a circuit is to operate as intended, a closed loop network must exist. Figure 3 illustrates a typical circuit. When a trace goes from source to load, return current must also be present, as required by both Kirchoff and Ampere. When the switch is closed, the circuit operates as desired. When the switch is opened, nothing happens. This on/off condition exists for both time and frequency domains. For the time domain, the desired signal travels from source to load and returns through a return path (Kirchoff's Law). In the frequency domain, RF current must also travel from source to load and return by the lowest *impedance* path possible.

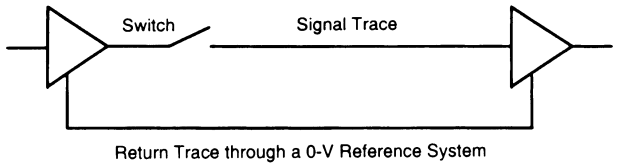

Figure 3. *Closed Loop Circuit.*

To eliminate undesired RF currents within a PCB (AC signal in nature, while the signal of interest is at a DC potential level) two important words need to be discussed: flux cancellation. If we cancel unwanted magnetic lines of flux, then radiated or conducted RF currents cannot exist. The concept of implementing flux cancellation is simple; however, one must be aware of many pitfalls and oversights that can occur when implementing flux cancellation techniques. With one small mistake, many additional problems will develop for the EMC engineer to diagnose and debug.

Before a detailed discussion of how return planes work is presented, common-mode (CM) and differential-mode (DM) currents are examined. Figure 4 illustrates CM and DM currents as they exist within a PCB.

In Figure 4, current source I_1 represents the flow of RF current from source E to load Z. Current flow I_2 is RF current observed in the return path. RF energy from common-mode currents is the sum of I_1 and I_2. For differential-mode RF currents, the field component is the difference between I_1 and I_2. If $I_1 = I_2$ exactly, differential-mode RF currents will not be present; hence, EMI will not exist. This occurs if the distance separation between I_1 and I_2 is electrically small. Common-mode currents are the main source of EMI. Differential mode currents are rarely observed as a radiated electromagnetic field.

An RF current return path is best achieved with an optimal (low impedance) return path. RF return current will approach zero (flux cancellation). However, if the return path is not provided through a path of least impedance, residual common-mode RF currents will be created. There will always be a finite amount of common-mode currents in a PCB trace since a physical, finite distance spacing will be present between the signal trace and return path (flux cancellation approaches 100%). The portion of the differential-mode return current that does not get canceled out becomes residual RF common-mode current.

The objective in a PCB layout is to have minimal impedance in the RF current return path. If we have a low impedance return path, differential-mode RF currents will be also be minimized. An example of a return path is shown in Figure 5. A multi-layer board with solid power and ground plane provides for excellent flux cancellation. Ground traces usually do not provide optimal flux cancellation under certain conditions. This is because the distance spacing between a clock trace and a ground trace may be physically greater than the distance spacing between the clock trace and the RF reference return plane.

For a reference plane to be effective, *no traces can be located in this solid plane.* Violations can exist only when a PCB layout designer understands how to accommodate this violation using specialized routing techniques. If a signal trace, or even a power trace (e.g., +12-V trace in a +5-V plane) is routed in a solid plane, this solid plane becomes fragmented into smaller parts. Provisions have now been made for an RF signal return loop to exist. Magnetic fields are propagated by loop antennas. This loop occurs by not allowing RF current in the signal trace to seek a straight line path (low impedance) back to its source. Split planes can now no longer function as a optimal return plane to remove RF currents.

A plane violation occurs when a clock trace is routed over a moated area. A moat is an absence of copper on all power and ground planes of a PCB. If a trace is routed over a moat, the RF current return path is not direct back to the source, and an RF current loop will be created causing radiated EMI. This is detailed in Figure 6.

Common-mode RF currents are generally observed in I/O interconnects. Rarely is common-mode noise observed internal to the PCB. Differential-mode currents can also be created as a result of a voltage gradient IZ drop that occurs between two points sharing the

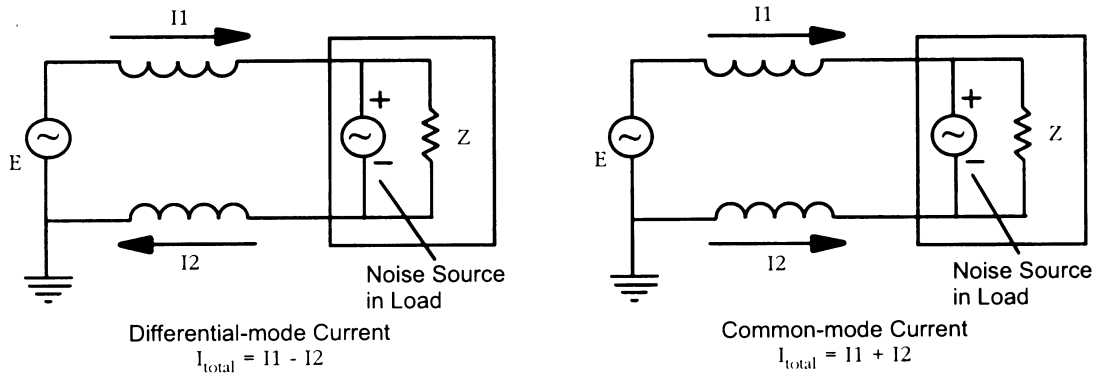

Figure 4. *Common- and Differential-mode Configurations.*

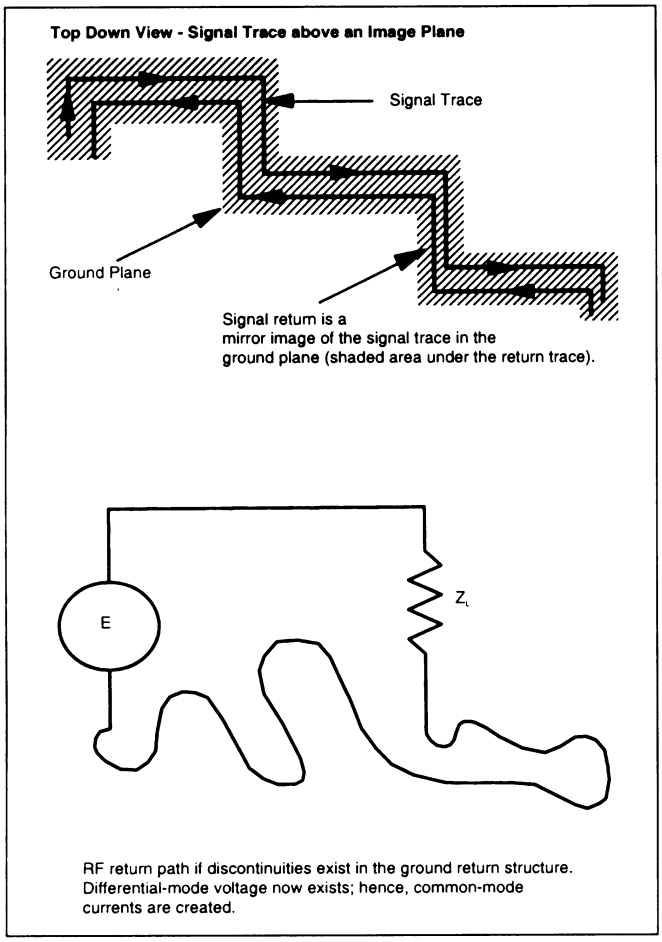

Figure 5. *Image Plane Concept.*

same 0-V reference. With an IZ drop, ground noise voltage is induced between these two circuits.

To implement flux cancellation within a PCB using reference planes, it becomes mandatory that critical nets with large RF spectral energy be adjacent to a solid RF return plane, preferably at 0-V (ground) potential. Ground planes are preferred over power planes because various logic devices may be quite asymmetrical in their pull-up/pull-down current ratios. These switching components may not present an optimum condition for flux cancellation due to signal flux phase shift, greater trace inductance, poor impedance control and noise instability. The ground plane is also preferred because this is where heavy switching currents are shunted. TTL asymmetric drive is heaviest to ground, with less current spikes to the power plane. For Emitter Coupled Logic (ECL), the more noisy current spikes are to the positive voltage rail. For CMOS, both power and ground reference are equal.

Examples of typical stackup assignments are shown in Figure 7. Stackup assignments for specific designs will be different due to the number of routing layers, power and ground planes required, or special engineering design requirements. Adjacent to each 0-V reference (ground) plane is a signal routing plane that must contain all clocks and other traces rich in RF energy.

Generally, a one- or two-layer PCB will not contain a ground or 0-V reference plane. As a result, optimal flux cancellation cannot occur. For a single- or double-sided stackup, each clock trace or sensitive circuit must be completely surrounded by a separate trace at 0-V reference potential. This 0-V reference trace must be connected to the 0-V reference from the power supply. The ground trace must also be located as close to the signal trace as physically possible based on the manufacturing process used to fabricate the board. This ground trace thus provides an alternate return path for RF currents to return to their source if a solid ground plane is not provided.

Bypassing and Decoupling

Capacitors are used for various functions within a PCB. Some of these functions include minimizing ground bounce, shunting RF energy between functional areas and I/O interconnects, and removing common-mode and differential-mode RF currents from a circuit. Capacitors not only prevent RF emissions from being created, they assist in minimizing externally-induced RF fields from entering the product (immunity protection). Before we examine how capacitors work, a definition of three different uses for capacitors is provided. Capacitors are used in one of three configurations; decoupling, bypassing and bulk.

Decoupling capacitors remove RF energy generated from high frequency switching components. They provide a localized source of DC voltage for devices or components, and are particularly useful in reducing peak current surges from being propagated across the PCB.

Bypassing capacitors remove unwanted RF noise that couples component or cable common-mode EMI into susceptible areas. They also provide other functions of filtering, as they are bandwidth limited.

Bulk capacitors maintain constant DC voltage and cur-

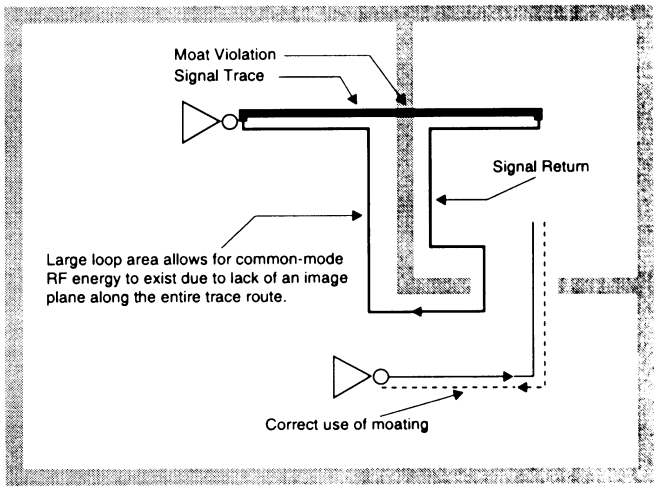

Figure 6. *Moating Concept.*

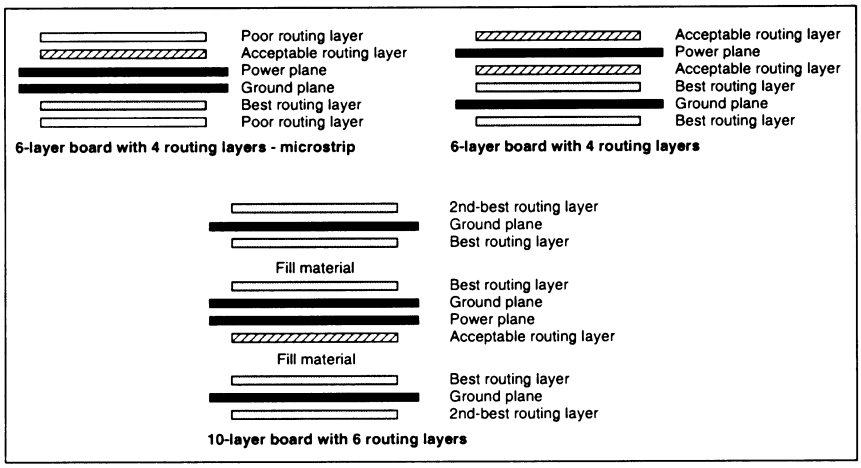

Figure 7. *Sample Stackup Assignments.*

rent to components when all signal pins switch simultaneously under maximum capacitive load. Bulk capacitors prevent power dropout due to dI/dt current surges generated by components consuming voltage and current within the power distribution system.

Restated, bypassing and decoupling refers to the prevention or propagation of RF energy from one area to another. These areas are power and ground planes, components, and internal power connections to I/O connectors. Bulk capacitors provide DC power to components to prevent a momentary voltage drop from occurring when a power supply is not located in the vicinity of the switching device.

Decoupling provides a localized source of charge for the proper operation of components during clock or data transitions, especially when all signal pins switch simultaneously under maximum capacitive load. Decoupling is accomplished by ensuring there is a low-impedance power source present in the power distribution system. Because decoupling capacitors have decreasing impedance (ability to remove RF switching currents) as the frequency increases up to the point of the capacitor's self-resonant frequency, high frequency noise is effectively removed from the power distribution system while low frequency RF energy remains relatively unaffected. All capacitor values and dielectric material must be chosen based on desired performance; they cannot be left to random choice from past usage or experience.

Capacitors consist of an *LCR* circuit with *L* (inductance in the lead length), *R* (resistance in the leads) and *C* (capacitance). A schematic representation of a capacitor is shown in Figure 8. At a known frequency, the series combination of *L* and *C* becomes resonant, providing very low impedance and effective RF shunting at resonance. At frequencies above self-resonance, the impedance of the capacitor becomes increasingly inductive and bypassing or decoupling becomes ineffective. Hence, the lead lengths of capacitors (surface mount, radial or axial), including trace length between a component and the capacitor, vias in the circuit, and the like, affect operational performance. Lead length inductance is an important parameter to consider when selecting capacitors for bypassing and decoupling. Other important parameters are the dielectric material and the tolerance rating of the capacitor.

If a capacitor must be used for a particular application, the question that exists is how to properly select this capacitor and how to incorporate it into the design.

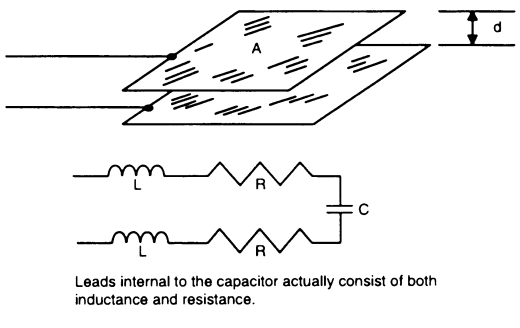

Figure 8. *Physical Characteristics of a Capacitor.*

DECOUPLING CAPACITORS

Components that switch logic states must be RF decoupled. This is because the switching energy generated by logic components will be injected into the power distribution system. This switching energy will be transferred to other logic circuits or subsections as common-mode and/or differential-mode RF noise. Typically, one selects a capacitor with a self-resonant frequency in the range of 2 - 100 MHz for circuits with edge rates of 2 ns or less (slower speed components). Typical multilayer PCBs are self-resonant in the 150 - 300 MHz range. Proper selection of decoupling capacitors, along with knowing the self-resonant frequency of the PCB assembly (acting as one large bulk capacitor) will provide enhanced EMI suppression of digital switching noise. Surface mount devices have a higher self-resonant frequency by up to two orders of magnitude (or 100). This higher self-resonant frequency is due to less lead length inductance. Aluminum electrolytic capacitors are ineffective for high-frequency decoupling and are best suited for power supply subsystems or power line filtering.

In addition to bypassing, high-frequency RF decoupling must always be provided in all clock generation areas. To do this, calculate the decoupling capacitance value to suppress RF switching noise for all significant clock harmonics. Choose a capacitor with a self-resonant frequency higher than the clock harmonics requiring suppression, generally

considered to be the fifth harmonic of the original clock frequency. In addition to this selection criteria, one must be cognizant of the amount of energy the capacitor provides to the component for proper operation.

Decoupling capacitors ideally should be able to supply all the DC current necessary during a state transition. Calculation of the local point-source charge of the decoupling capacitor is represented by Equation 1. This equation does not calculate self-resonant frequency, only the localized source charge required to remove RF switching noise from the power distribution system. As observed, use of 0.1-µF capacitors in today's products are usually insufficient for optimal decoupling when the edge rate of the device is faster than 5 ns. Use of decoupling capacitors on two layer boards is, however, required to reduce power supply ripple. Decoupling capacitors for low frequency applications are usually not needed when multilayer boards are used, given that the capacitance between the power plane and ground planes provides overall decoupling for low frequency or slower edge rate components and are more efficient than discrete components.

$$C = \frac{\Delta I}{\Delta V / \Delta t} \quad (1)$$

$$\text{i.e.,} \quad \frac{20\ \text{mA}}{100\ \text{mV} / 5\ \text{ns}} = 0.001\ \mu\text{F or } 1000\ \text{pF}$$

where
C = Capacitance
I = Current transient
V = Allowable power supply voltage change (ripple)
t = Switching time

When selecting decoupling capacitors, in addition to providing a localized source charge, calculate the self-resonant frequency based on the actual edge rate of the logic family used, not a manufacturer's data book value; the real, unpublished edge rate. Equation 2 provides for calculating the self-resonant frequency of a capacitor. Be aware that inductance is a part of this equation. Lead length inductance is not intuitively known, and is usually an unknown constant.

$$\omega = 2\pi f = \sqrt{\frac{1}{LC}} \quad (2)$$

A capacitor remains capacitive up to its self-resonant frequency. Above self-resonance, the capacitor becomes inductive and ceases to function for RF decoupling. This is observed in Figure 9. Placement of the capacitor should also be as close to the component pin as physically possible to minimize lead length inductance if a multilayer board is not provided. It is common practice to use a 0.1-µF capacitor for decoupling high technology PCBs which is a poor choice in today's high-technology, high-speed systems. This 0.1-µF value was selected in 1965 by the USA military to decouple 20-kHz components. Components used in today's products now require decoupling in the range of 0.01-µF to 100 pF. Again, capacitance value and lead length inductance determines the self-resonant frequency and the amount of decoupling provided.

Another concern for selection of a decoupling capacitor is the dielectric material used to manufacture the device. Figure 9 shows the self-resonant plots of three different dielectric materials. The cost of using specific dielectrics is negligible, especially when EMI compliance is required and decoupling will assist in solving the emissions problem.

A benefit of using multilayer PCBs is the placement of the power and ground planes adjacent to each other which creates one large decoupling capacitor, generally in the range of 150-300 MHz. This internal decoupling capacitor usually provides adequate decoupling for slow speed (slow edge rate) designs. If components have signal edges (*tr*) slower than 10 ns (e.g., standard TTL logic), use of low, self-resonant frequency decoupling capacitors is generally not required as the majority of decoupling is performed by the internal power and ground planes. Bulk capacitors, however, are still needed to maintain proper voltage levels for performance reasons. Above the upper limit of decoupling provided by the power and ground planes, discrete capacitors must still be used for operation above 300 MHz.

BYPASS CAPACITORS

Bypass capacitors are commonly used to divert common-mode RF currents that are present on cable shields by creating an AC short to chassis ground. RF currents are, in reality, an AC component (sine wave). Bypass capacitors must be placed where I/O interconnects attach to the PCB. If the braid of the cable is floating, or not bonded to chassis ground, a bypass capacitor is required to remove common-mode currents present on the cable shield from either

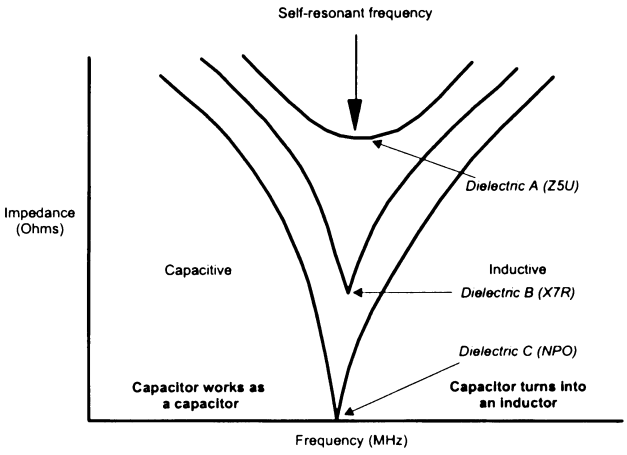

Figure 9. *Dielectric Material and Self-resonant Frequency of Same Value Capacitors.*

radiating into free space or causing a disruption to the chassis due to an immunity event. Again, short lead lengths are a primary design consideration. When selecting bypass capacitors, proper bandwidth filtering and peak surge voltage protection capabilities for electrostatic discharge (ESD) protection should be kept in mind.

Another item to remember for ESD protection is to use bypass capacitors with a high self-resonant frequency between the power and ground structure. These bypass capacitors must have as low an equivalent series inductance (ESL) and equivalent series resistance (ESR) as possible. Frequent use of bypass capacitors reduces loop areas between the power and ground planes for low-frequency, high-level ESD events. For higher-frequency ESD, standard value capacitors (i.e., 0.1 µF) become less effective due to both the capacitors' internal stray and interconnect trace inductance to the component or ground stitch location. Use of MOVs, transient suppression devices, spark gaps, diodes, etc., may also be required.

BULK CAPACITORS

Bulk capacitors maintain proper dc voltage and current to components when these devices switch all data, address and control signals simultaneously under maximum capacitive load. Large power consuming components will cause voltage fluctuations on the power distribution system. These fluctuations will cause improper circuit performance due to voltage sags, ground bounce and ground noise voltage. Bulk capacitors also provide large amounts of energy storage to maintain voltage and current requirements of switching components. Bulk capacitors play no significant role in EMI control.

Bulk capacitors, usually tantalum dielectric, must be used in addition to higher self-resonant frequency decoupling capacitors to provide DC power for components and to prevent power plane RF modulation. Place one bulk capacitor for every two LSI and VLSI components in the following locations:

- Adjacent to clock generation circuits
- At the power entry connector on the PCB
- At all power terminals on I/O connectors for daughter cards, peripheral devices and secondary circuits
- Near power-consuming circuits and components
- At the furthest location from the input power connector
- High density component placement remote from the DC input power connector

When using bulk capacitors, calculate the capacitor voltage rating such that the nominal circuit working voltage equals 50% of the capacitor's voltage rating to prevent the capacitor from self-destruction if a voltage surge occurs.

Conclusion

When examining how EMI is created in a PCB, various engineering aspects related to Maxwell's equations must be considered. The existence of magnetic lines of flux present within a transmission line structure is the primary cause of RF energy generated within the PCB structure. Other major areas of concern include the creation of common-mode and differential-mode currents between circuits and interconnects, ground loops creating a magnetic field structure between components and ground structures, and component radiation from a device package.

To reduce or eliminate unwanted RF energy, magnetic lines of flux must be removed. This is easily performed using flux cancellation techniques. The most common and easiest method is to provide a return path that is as physically close as possible to the offending transmission path to allow the closed loop circuit to become tightly coupled. This is best accomplished with return planes and traces at 0-V reference. Keeping the RF return path adjacent to the trace containing the flux is mandatory without routing the return path over gaps in the return plane.

One must differentiate between decoupling and bypassing when implementing suppression techniques on a PCB. Decoupling is provided at the component level to prevent ground-noise voltage and high frequency voltage spikes being injected into the power and ground plane structure. Differential-mode voltages create common-mode currents. It is common-mode currents that are measured as EMI emanating from a product. Bypass capacitors divert common-mode currents from I/O cables, thus allowing only the desired data stream to be present. Bulk capacitors keep the unit functioning by insuring that sufficient voltage is present for all circuits under maximum power consumption usage while assisting in preventing ground bounce from occuring.

Reference

1. Kimmel, B., and Gerke, D., *The Designer's Guide to Electromagnetic Compatibility*, EDN, January 20, 1994.

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Printed Circuit Board Suppression Concepts for EMC Compliance

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PART 2

THIS IS THE SECOND of a two-part article that presents fundamental EMC concepts related to designing suppression for EMC compliance into printed circuit boards (PCBs). Part 1 appeared in ITEM 1998. *Together, these two articles create one comprehensive document. Both articles present explanations of EMI and various design and layout techniques that are easily implemented. These techniques provide the reader with a fundamental understanding of how one can implement RF suppression during layout which will minimize EMI threats at the beginning of a design project. Topics examined in Part 1 included how and why EMI exists, image planes and stackup assignments, and bypassing and decoupling.*

Routing Clock Traces

To a significant degree, oscillators, associated components, and clock traces account for most of the emissions generated within a PCB. A clock circuit area is defined as the functional area that physically contains the oscillator, buffers, drivers and associated components, both active and passive. RF emissions are the result of both the rise and fall time (edges rate) as well as the fundamental clock frequency of digital components switching between logic states.

To determine the spectral distribution of RF energy that will be developed, use Equation 1. This equation does not take into account harmonics created from the primary frequency. A product design must take into consideration up to the tenth harmonic of the highest internally-generated frequency created within the PCB.

$$f_{max} = \frac{1}{\pi \cdot t_r} \qquad (1)$$

where

f_{max} = Maximum generated RF frequency range

t_r = Edge rate (rise or fall time—use the faster of the two)

For example, a 2-ns edge rate, typical of common clock drivers and components, can be expected to radiate significant RF energy up to 160 MHz, falling off rapidly above that frequency. The possible significant RF spectrum is $10 \cdot f_{max}$ or 1.6 GHz, which includes the harmonic content of the main frequency component.

To minimize emissions that may be created within a PCB, traces rich in RF energy should always be *manually* routed. After successful routing of these high threat traces, we may automatically route the remaining nets.

COMPONENT PLACEMENT

RF generating components should be located in an area of the PCB as close to, or adjacent to, a ground stitch location (to chassis ground if multipoint grounding is used), rather than along the perimeter or near the I/O section. If a trace with RF energy travels to a daughter card, ribbon cable, interconnect or the like, this clock circuit must be located some distance from this interconnect, but not so far away as to make the interconnect trace electrically long, which could cause a signal integrity problem.

For these single-ended traces, the clock trace must be terminated directly at the interconnect to prevent an open-ended transmission line. It is imperative that this be comprised of a single point-to-point connection. Termination of clock traces at interconnects guarantees signal quality when the connector is not provided. In addition, trace termination prevents excessive RF currents from coupling into other areas susceptible to RF corruption. Devices that create clock signals (oscillators, clock drivers, buffers and the like) must be installed directly on the PCB—do not use sockets! Sockets add lead length inductance to the trace (LdI/dt). Lead length inductance allows ground noise voltage to develop by creating a difference in reference voltage between two points. In turn, ground noise voltage generates common-mode RF currents, which will radiate or couple into susceptible areas.

TRACE LENGTHS

During layout, components that use clocks or periodic signals should be located such that the traces are routed for the shortest distance possible (minimal Manhattan length) with a

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minimal number of vias. Ground vias may, however, be required. These are discussed later. Vias add inductance to a trace (approximately 1-3 nH each). Inductance in a trace may cause functional signal quality concerns and potential RF emissions, as presented earlier. This trace inductance is added to the sum of the inductance of all vias and the bond wires internal to a component's package. The faster the edge rate of a clock signal, the more this design rule approaches mandatory status. If a periodic signal or clock trace must traverse from one routing plane to another (layer jump), this transition should occur only at a component lead at 0-V reference or ground, and not anywhere else. This is discussed later in the section on layer jumping (or use of ground vias). The goal is a maximum of two vias per route, one at the source, and one at the load, if a stripline configuration is provided.

The old directive to "keep clock lines short" will always be valid. The longer the trace, the greater the probability that RF currents will be produced, and a larger spectral distribution of RF energy created. Clock traces must be terminated to reduce ringing and creation of avoidable RF currents. This is because unterminated lines allow signal reflections to exist, which can also cause EMI to be created. Improperly terminated clock signals might also degrade the signal to the point of being nonfunctional.

Determining Electrically Long Trace Lengths

How do we determine if a trace is electrically long during component placement? A simple method exists that allows PCB designers to ascertain whether a trace requires termination or special treatment by the design engineer. The velocity of propagation within a trace is typically 60 percent the speed of light (based on the dielectric constant of the material used). The maximum permissible unterminated line length is calculated per Equation 2. This equation is valid when the two-way propagation delay (source-load-source) is greater than, or equal to, the signal rise or fall time from a source driver.

$$L_{max} = \frac{t_r}{2\, t'_{pd}} \qquad (2)$$

where

t_r = Edge rate of the transition (ns)
t'_{pd} = Propagation delay of 1" of line
L_{max} = Maximum round trip distance of the routed trace (centimeters)

When dealing with transmission lines, a PCB designer needs a quick rule-of-thumb during component placement that enables determination of whether a trace routed on a PCB is considered to be an electrically long trace. A simple calculation is available that approximates the length of a trace, to determine if it is electrically long, with a high degree of accuracy. When determining if a trace is electrically long, we must think in the time domain.

Equation 2 can be simplified as follows. Substituting the propagation delay of FR-4 material with a dielectric constant of 4.6 (at 10 MHz) for both microstrip (1.72 ns/ft) and stripline (2.26 ns/ft), use two simple, basic equations to calculate the maximum electrical line length before termination is required. The equations take into account the conversion from feet to centimeters. If the round trip, routed trace length is greater than L_{max}, then both signal functionality and EMI concerns exist. Figure 1 illustrates this equation for quick reference.

L_{max} = 9 • tr (for microstrip topology, in cm.) (3)
L_{max} = 3.5 • tr (for microstrip topology, in in.)
L_{max} = 7 • tr (for stripline topology, in cm.) (4)
L_{max} = 2.75 • tr (for microstrip topology, in in.)

For example, if a signal transition is 2 ns, the maximum unterminated trace length when routed microstrip is:

$$L_{max} = 9 \bullet tr = 18 \text{ cm } (7").$$

When this same trace is routed stripline, the maximum unterminated length of this 2-ns transition is:

$$L_{max} = 7 \bullet tr = 14 \text{ cm } (5.5").$$

If a trace is longer than L_{max}, termination should be implemented, as signal reflections (ringing) will occur in this electrically long trace. Ringing created by an impedance mismatch

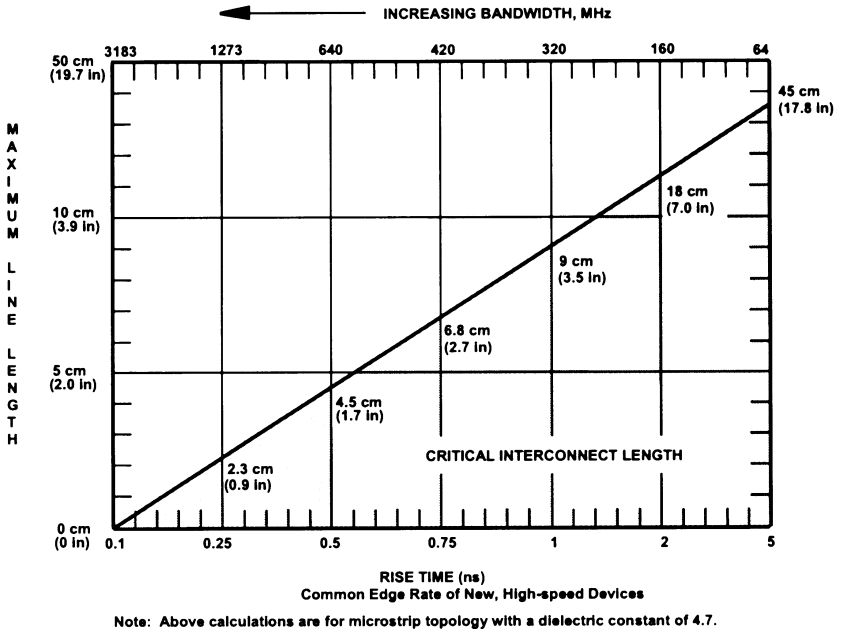


Figure 1. *Maximum Unterminated Line Length Vs. Signal Edge Rate (FR-4 Material).*

in an electrically long trace may also make the circuit non-functional, and could create RF currents within the trace (common-mode). Even with good termination, a finite amount of RF current will still be present within the trace.

For every signal, a time domain reflection occurs. There will always be a finite time period for a signal to travel from source to load, and then return from the load to source. An electrically long trace is a trace that allows the one-way (source to load) propagation delay to exceed ½ the clock cycle. If a second clock signal (edge transition) occurs before the reflection of the original reflected signal returns to the source, ringing will develop. Depending on the phasing of the reflection, overshoot or undershoot may occur, which will cause significant signal quality issues to be present. Signal degradation is a concern if the edge time of the signal constitutes a significant percentage of the propagation time between the device load intervals.

Routing Layers

A frequent concern is how to determine on which layer or planes clocks or periodic signals are to be routed. Clocks and periodic signals must be routed adjacent to a solid reference plane, preferably at ground or 0-V potential, not floating. This is true for both routing layers, x axis and y axis, also identified as the horizontal or vertical routing planes. Several issues must be remembered when selecting routing layers. These issues include which layers to use for trace routing, jumping between designated layers and maintaining a constant trace impedance throughout the trace route.

Figure 2 illustrates how to optimally route clock traces on different layers, assuming a multilayer stackup.

- A solid reference (image) plane must be used adjacent to the signal trace. Minimize routed trace lengths while maintaining a constant trace impedance (constant trace width). If series termination is used, connect the resistor directly to the output pin of the component. After the resistor, place the via internal to the stripline layers.
- Do not route clock or sensitive traces microstrip if a six or more layer stackup is provided. The outer layers of the PCB should be reserved for large signal buses and I/O circuitry that does not create RF energy. When routing traces between layers, there may develop a change in the characteristic impedance of the trace (trace to reference plane), thus affecting performance and possible signal degradation.

If a constant trace impedance is maintained, and the use of vias is minimized or eliminated, the trace will not radiate any more than a coax.

Layer Jumping (Use of Ground Vias)

When routing clocks or high-threat signals, we generally via the trace down to a routing plane (e.g., x axis) and then via this same trace to another plane (e.g., y axis) from source to load. This is shown in the poor routing method of Figure 2. It is generally assumed that if each and every trace is routed adjacent to an image plane, there will be tight RF coupling between the signal trace and reference plane (flux cancellation). In reality, this assumption is incorrect.

When a jump is made from a horizontal to a vertical routing layer, the RF return current cannot make this jump. The return current must now find an alternate, low impedance path to complete the closed loop boundary requirements. This alternate return path usually does not exist when jumping a trace between layers. To minimize creation of EMI and crosstalk due to layer jumping, the following design techniques have been found to be effective.

- Route all clock and high-threat signal traces on only one routing layer.
- Verify that a solid 0-V reference, or ground plane, is adjacent to the routing layer with no discontinuities in the route, e.g., plane cuts or moats.
- If a via must be used for routing a sensitive (high-threat or clock) signal trace between the horizontal and vertical routing layer, incorporate corresponding ground vias at each and every via location where the axis jumps occurs.

A ground via is a via that is placed directly adjacent to each signal route

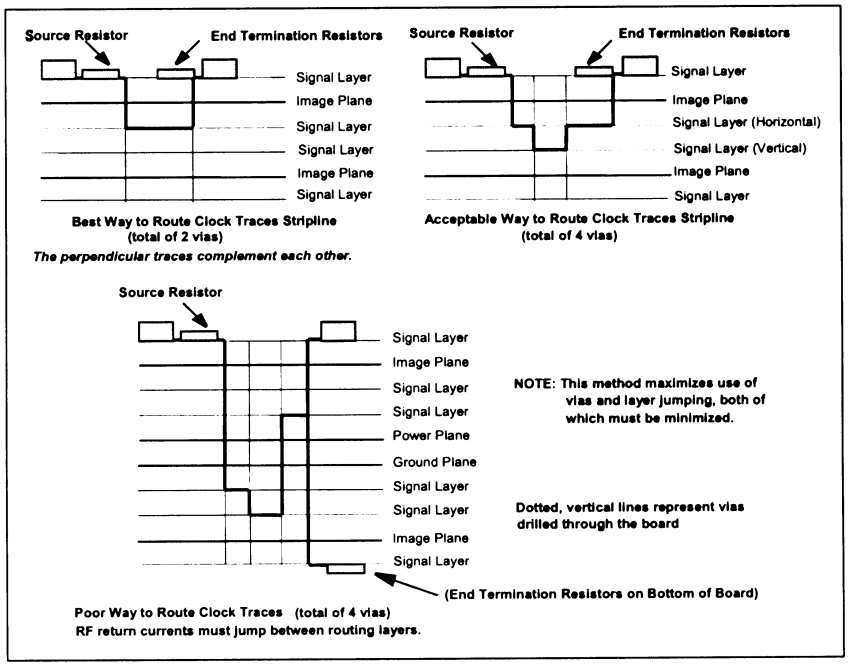


Figure 2. *Routing Clock Traces.*

via. Ground vias can only be used when there are multiple ground planes in the PCB. This via must connect all the ground planes together. Ground vias allow for a constant RF image plane return path to be present adjacent to a signal route, and provide a mechanism for optimal flux cancellation. The ground pin of a component (pin escape or breakout) makes an excellent ground via.

Impedance Control and Trace Termination

Trace termination assists in the reduction of RF energy in addition to insuring signal functionality and quality for performance reasons. In order to achieve optimal termination, the impedance (Z) of the trace or transmission line must be maintained within a certain percentage of its desired value. Typically, a trace will have an impedance between 45 and 120 ohms depending on how the PCB is constructed. In this section, we examine several methods of controlling the impedance of a trace within a PCB and discuss commonly-used termination methods for various applications.

Impedance Control

With today's high technology products and faster logic devices, transmission line effects become a limiting factor for proper circuit operation. A trace routed adjacent to a reference plane forms a simple transmission line. A trace does not contain voltage, current or electrons. A trace transfers an electromagnetic field from source to load. To guarantee that the electromagnetic field does not incur a loss during transmission, or to allow signal reflections to be created, both the source and load impedance must be matched (maximum power transfer theorem). The major parameters describing transmission line impedance is trace width, distance spacing between the trace and reference plane and dielectric constant of the PCB material.

Impedance Calculations

The popular formulas used for microstrip and stripline were first published in the Motorola MECL System Design Handbook HB 205. Motorola popularized this formula set in the 1970's in conjunction with its ECL logic family. When these equations were published, the impedance was assumed to be in excess of 75 ohms, with traces 0.020-inch thick and a height separation of 0.020-inch between trace and reference plane. As a result, these commonly-published formulas achieve accuracy within a tolerable range for a majority of product designs.

Today's products, however, are commonly fabricated at 0.005 inches or less. With such close trace-to-plane separation, effects of the reference plane related to the trace become pronounced. These equations fail to provide accurate answers when low-impedance clock distribution traces are provided (i.e., 20 ohms).

We must maintain trace impedance at a constant value throughout the entire route. Depending on application, impedance tolerance levels may differ by +/-10%. Vias within a trace route, (at approximately 1-3 nH inductance and 2-pF capacitance each) may cause the overall impedance of the trace to change from a desired value by the equation $Z = \sqrt{L/C}$. For critical signals, an impedance discontinuity in the transmission path may cause functionality concerns (time domain). In addition, vias prevent RF return currents from finding a low impedance return path back to their source whenever a trace changes a routing layer (layer jumping). Layer jumping is a primary cause of EMI, as a continuous return path for RF return currents will not be present.

When developing a stackup assignment, determine the trace impedance desired prior to routing any trace. Selecting a proper trace width is necessary to maintain a constant impedance throughout the trace route. For example, for a symmetrically-balanced 6-layer PCB, 0.010-inch trace width, and dielectric constant $\epsilon r = 4.3$, we have 66-ohm impedance for embedded microstrip and a 97-ohm trace for outer microstrip. Using this example, if traces are jumped between routing layers with different impedances, a standing wave ratio (SWR) of 1:1.5 occurs. If the length of the trace is significant, functionality concerns become dominant, not EMI.

When a trace jumps layers, such as stripline to microstrip, with a 1:1.5 mismatch, a simple design technique to maintain constant impedance is to change the routed trace width on different layers. For the example above, the outer microstrip trace should be 32 mils (0.032") wide while the embedded microstrip trace is 12 mils (0.012") wide for a constant 55 ohm transmission line. Although easy to implement, changing the width of selected traces on a routing layer is a design concept that is usually not implemented for various reasons. This is because a PCB designer, or the layout specification requirement, mandates all traces within the PCB to be the same width for consistency, especially if an autorouter is used. In addition, less room exists for routing many traces' outer microstrip if wide trace widths exist. The concept of maintaining the same trace width for all traces in new, high-speed, high-technology designs is now an outdated concept.

Trace Termination

It is common practice to daisy chain periodic signal and clock traces for ease of routing. Unless the routed distance is small between loads, (with respect to the propagational delay of the routed trace), signal reflections may occur. Daisy-chaining affects signal quality sometimes to the point of non-functionality. Therefore, *radial* connections for fast edge signals and clocks are preferred. Examples of these two routing methodologies are shown in Figure 3.

If a clock trace must be electrically long, and it contains edge transitions faster then 2 ns, the trace should be routed as a transmission line. Use of a transmission line structure mini-

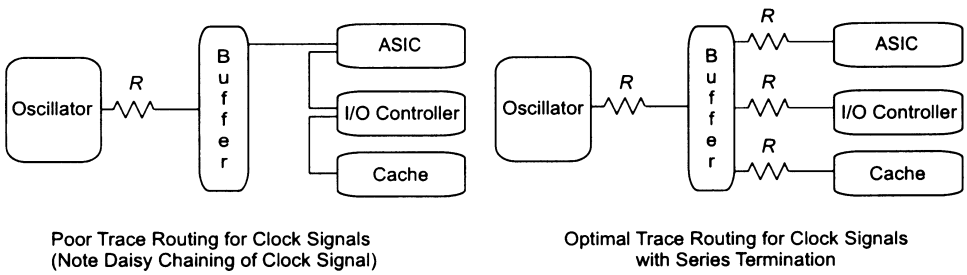


Figure 3. *Termination of Clock Traces.*

mizes ringing and reflections (signal integrity concerns). In addition, we maintain a constant impedance for the trace. Ideally, trace impedance should be kept at 10% of nominal value. In some cases, 20% to 30% is acceptable only after careful consideration is made as to whether signal integrity will be affected by this larger tolerance level.

To assure optimal signal quality, trace termination may be required. There are five termination methods commonly used. These methods are dependent on the complexities of the layout geometry, component count, power consumption and other items detailed below. When a source driver is overloaded, termination can degrade the transmitted signal if incorrectly specified or implemented.

Five commonly-used termination methods are listed below and detailed in Figure 4.

1. Series termination resistor
2. Parallel termination resistor
3. Thevenin network
4. RC network
5. Diode network

Series Termination Resistor

Series termination is optimal with a single source driver and single load. Use the series resistor when the output impedance of the driver, ($Z_{output\ driver}$) is less than the loaded characteristic impedance of the trace (Z_{trace}). In other words, $R_s = Z_{trace} - Z_{output\ driver}$. Locate the resistor directly at the output of the driver without the use of a via between the two, if at all possible.

- When the output impedance ($Z_{output\ driver}$) plus series resistor (R_s) equals the characteristic impedance of the trace (Z_{trace}), the voltage waveform at the output of the resistor is divided evenly with half of the voltage transmitted to the receiver. If the receiver has a very high input impedance, the full waveform will be observed immediately, while the source will receive the reflected waveform at 2 • tpd (round trip propagation delay). Since devices have different input and output impedances, especially the source driver, use of a series resistor may not be optimal.

Parallel Termination Resistor

For parallel termination, a single resistor is provided at the end of the trace route. This resistor, *R*, must have a value equal to the impedance of the trace or transmission line. The other end of the resistor is tied to a reference source, usually a ground. Parallel termination may add a small propagation delay to the signal due to a combination of both resistance and distributed capacitance within the transmission line structure.

A disadvantage of parallel termination is consumption of DC power, since the resistor is generally in the range of 50 ohms to 150 ohms. The driver must source current when driving the trace logic high. In applications where power consumption is critical, e.g., battery-powered products (notebook computers, for example), parallel termination is a poor choice. An increase in drive current will cause an increase in power consumption from the power supply, an undesirable feature in battery-operated units.

Thevenin Network

Thevenin termination has one advantage over parallel termination. One resistor is connected to the power rail, the other resistor to ground. Unlike parallel, Thevenin allows for optimizing the voltage transition point between logic HI and logic LOW. When using a Thevenin network, consideration in choosing the resistor values must be made to avoid improper setting of the voltage reference level for both logic HI and LOW. The ratio of R1/R2 also determines the relative proportions of logic HI and LOW drive current. The Thevenin equivalent resistance must be equal to the characteristic impedance of the trace. Like parallel termination, Thevenin consumes power as the source driver must either sink or source current on the trace at all times.

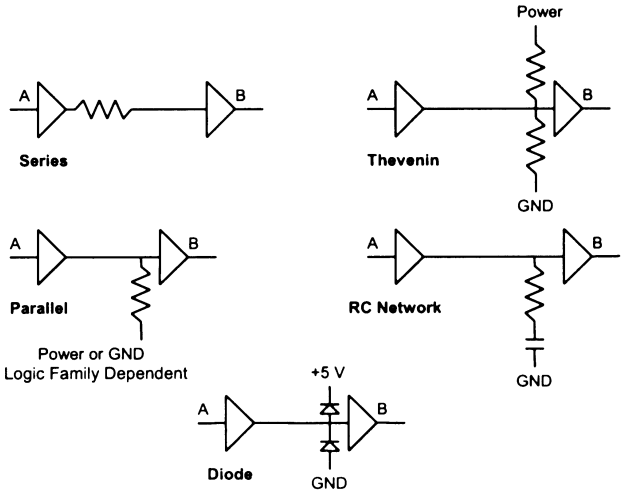


Figure 4. *Termination Methodologies.*

RC Network

The RC network (also known as AC) works well in both TTL and CMOS systems. The resistor matches the characteristic impedance of the trace (identical to parallel). The capacitor holds the DC voltage level of the signal. The source driver does not have to provide drive current to the terminating network. As a result, AC current (RF energy) flows to ground during a switching state. The capacitor allows RF energy (which is an AC sine wave component, not the DC logic level of the signal), to pass through to a 0-V reference. Although an additional propagation delay is presented to the signal due to the RC time constant, less power dissipation exists over parallel or Thevenin termination. From the viewpoint of the circuit, all three end termination methods are identical. The main difference lies in power dissipation, with RC consuming far less power than the other two.

The termination resistor must equal the Zo of the trace while the capacitor is generally very small (20-600 pF). The RC time constant must be greater than twice the loaded propagation delay (round trip travel time). RC termination finds excellent use in buses containing similar layouts.

Diode Network

The diode termination method is commonly used for differential or paired networks and analog devices. Diodes are used to limit overshoot and undershoot while providing low-power dissipation. The major disadvantage of diodes lies in their frequency response to high-speed signals. Although overshoots and undershoots are prevented at the receiver's input, reflections will still exist, as diodes do not affect trace impedance or enhance signal functionality. To gain the benefits of both techniques, diodes may be used in conjunction with the other methods discussed herein to minimize reflection problems.

Miscellaneous Suppression Techniques

There is more than one way to design and layout a PCB. All techniques presented here have a proven track record for preventing the creation of RF energy, reducing common-mode currents created from component switching logic states, and preventing ground loops in the RF return path from occurring.

Items presented include the 20-H rule, the 3-W rule, moating and isolation, and grounded heat sinks.

20-H Rule

Between the edges of the power and ground planes in a multilayer PCB, magnetic lines of flux link the two planes. This interplane coupling is called fringing and is generally observed on only very high speed PCBs. When using high-speed logic and clock circuits, the power and ground planes can couple these flux lines to each other, thus radiating RF energy into free space. To minimize this coupling effect, the power planes must be physically smaller than the closest reference ground plane per the 20-H rule. Figure 5 shows the effects of RF fringing from the edges of a PCB.

To implement the 20-H Rule, calculate the physical spacing (distance) between the power plane and its nearest ground plane. This distance includes the thickness of the core or prepreg material. If a distance separation of 0.006 inches is assumed to exist between the two planes, calculate "H" as (20 • 0.006 inches) = 0.120 inches. Physically make the power plane 0.120 inches smaller than the ground plane on all four sides if the straight line distance along the edge of the PCB exceeds $\lambda/20$ of the higher generated frequency within the PCB. If a power pin to a component is located within this isolated area (absence of copper), the power plane may be jogged to provide power to this isolated pin. This is detailed in Figure 6. What we are concerned with is the linear straight-line distance along the edge between the planes. Any linear length between the parallel plates acts as a resonant antenna based upon the physical length of the driven elements relative to the fre-

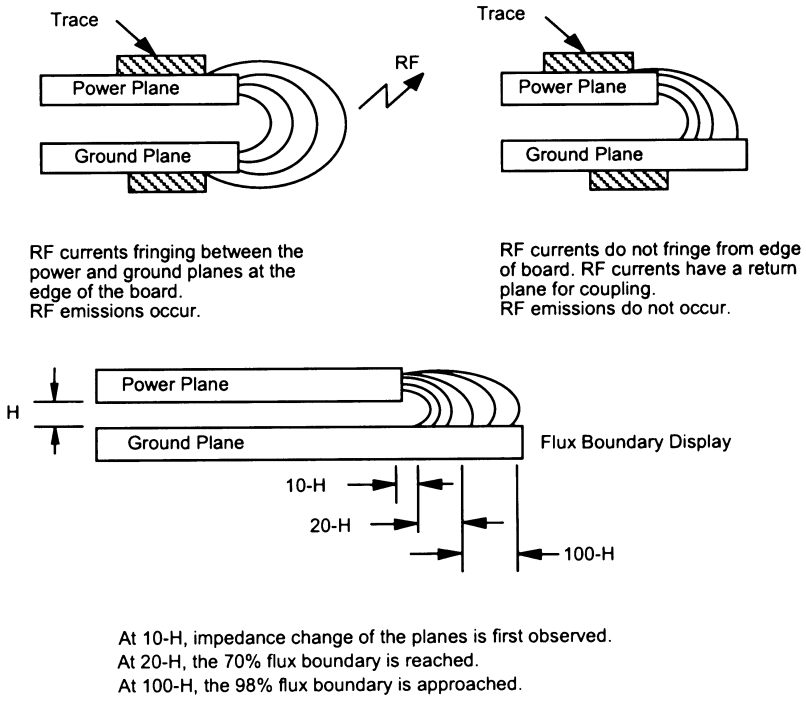


Figure 5. *Concept of the 20-H Rule.*

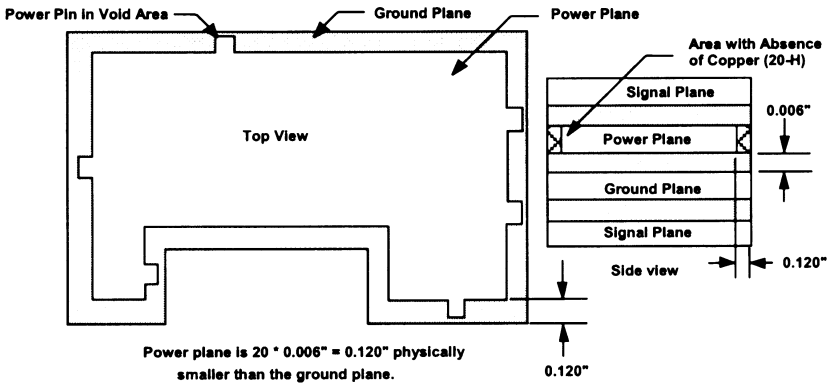


Figure 6. *Implementing the 20-H Rule.*

quency of RF energy that exists within the power and ground planes.

When using the 20-H Rule, signal traces routed adjacent to the power plane must be rerouted inward to be physically adjacent to the solid reference (power) plane, not over the absence of copper area. There can be no exceptions. It becomes important for the PCB designer to examine all planes individually for proper implementation and to verify 20-H of the power plane and to guarantee that traces are physically adjacent to a solid RF return path or plane.

3-W Rule

Use of the 3-W rule is required to minimize coupling between traces rich in RF energy. The 3-W rule states that "the separation distance between traces must be three times the width between traces measured from centerline to centerline." Otherwise stated, "the separation distance between two traces must be greater than two times the width of a single trace." For example, a trace is 0.006 inches wide. No other trace can be physically located within 0.012 inches of this trace, edge-to-edge. As observed, much real estate is lost in areas where trace isolation occurs. An example of the 3-W rule is shown in Figure 7.

The advantage of using the 3-W Rule is that it assists in the reduction or elimination of crosstalk between signal traces. Crosstalk occurs when RF flux created in one trace couples onto an adjacent trace. Details of the actual mechanism is beyond the scope of this article. Design engineers generally simulate a PCB layout to determine if crosstalk exists. Use of 3-W can save the design engineer many hours of extensive simulation analysis if time does not permit for computer simulation. Clock traces and high threat signals are prime candidates for mandatory use of 3-W.

Isolation and Moating

Isolation refers to the physical separation between components, circuits and power planes from other devices, functional areas, and subsystems. Allowing RF energy to propagate to different parts of the PCB by radiated or conductive means will cause problems not only in terms of EMI, but also with regard to functionality.

Isolation is created by absence of copper. Absence of copper is a wide separation (typically 25 mils minimum) within all solid planes of the PCB. In other words, an isolated area similar to an island in the middle of the board is created. Only those traces required for operation or interconnect can travel to or through this separated area.

The area characterized by absence of copper is also identified as a moat. A moat serves as a keep-out zone for signals and traces that are unrelated to the moated area's function or its interface. An example of a moat for an I/O connector is shown in Figure 8. It is common to implement moating in the middle of a PCB to separate a clock generation circuit from non-related components susceptible to RF corruption through common-impedance coupling of the power and ground planes. Moated areas include analog-to-digital partitions, I/O interconnects and similar applications.

The reason we implement partial moats in the middle of a board is to force RF return currents to travel a specific path to a chassis ground location through the path of least impedance. We control the flow of RF return current by forcing it to take a predetermined path to ground per our design requirements, not leaving this to chance. If a moated area is separated from other sections of the board,

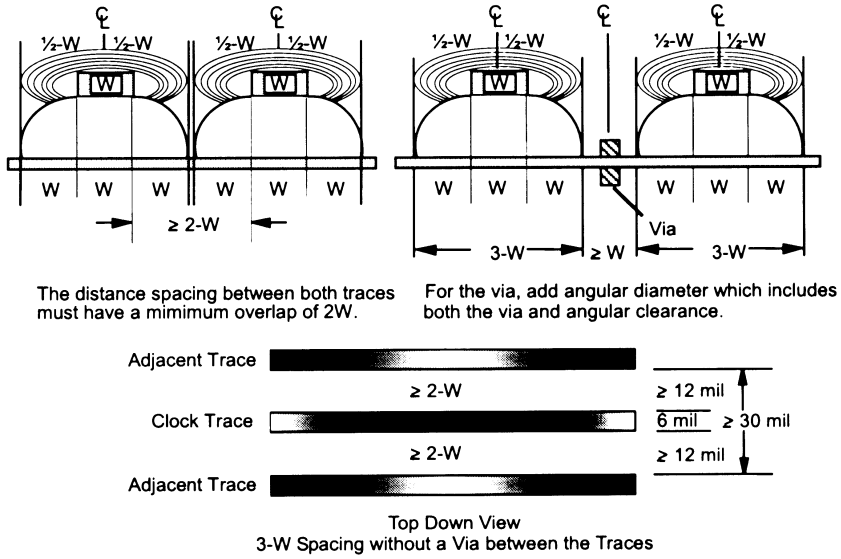


Figure 7. *Implementing the 3-W Rule.*

this isolated zone keeps its internally-generated RF ground noise to itself. Generally, moated areas are small enough to not cause RF currents to be created. We also want to prevent clock generation circuitry from coupling their RF currents into nearby I/O connectors and other circuits susceptible to RF corruption.

If we moat or isolate an area 100 percent, then how does one cross this moat with traces? Three methods exist:

- Route all traces across the moat on only one side of the circuit area to prevent RF return currents from creating a ground loop through two sides of the moat.
- Cross the moat with a ferrite bead-on-lead or common-mode choke.
- Route all traces through a bridge.

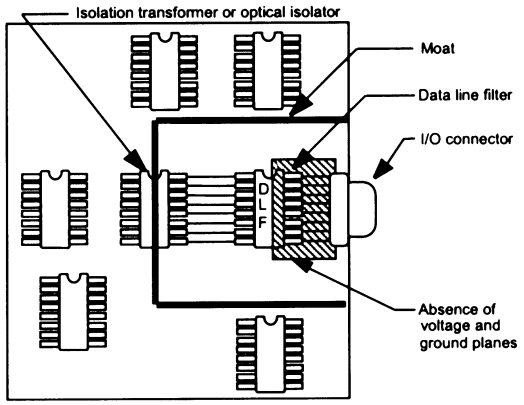
Bridging is shown in Figure 9. Note that all signals that travel from the main section to the I/O area pass through a bridge or opening in the moat. No trace must cross the moat under any condition! The RF current return path must be physically next to the routed signal trace to cancel out magnetic lines of flux that exist between the two. If a moat violation occurs, the RF return current must take a longer path home, which allows for the creation of undesired, common-mode RF current.

In addition to minimizing the RF return path, ground return currents can be easily directed into the ground reference system. A ground point must be located close to the bridge opening, so it can source RF currents to chassis ground if multipoint grounding is provided. Optimal sourcing of RF currents to a 0-V reference keeps ground plane noise from corrupting other functional areas, or I/O interconnects, by common-impedance coupling.

Grounded Heat Sinks

Grounded heat sinks are a new concept in PCB suppression that finds use in specific applications and for certain components. Grounded heat sinks are sometimes required when using processors with internal clocks in the 75 MHz range and above, or for components that create large amounts of common-mode currents internal to the device package. These devices require more extensive high-frequency decoupling and grounding than most other parts of a PCB.

RISC processors or VLSI components usually have a high internal self-resonant frequency. This high self-resonant frequency is a combination of the manufacturing process and internal clock speed. As a result, these components can radiate RF energy more so than most other components, even clock traces, if RF suppression techniques are not incorporated by the component manufacturer. Any attempt to remove this radiated RF energy, using standard suppression techniques, is nearly impossible, except through the use of a heat sink as a common-mode decoupling capacitor. The heat sink is used in addition to the standard differential-mode decoupling capacitors normally provided. A common-mode decoupling capacitor provides an AC shunt to remove common-mode energy within a device package, transfering this energy into a 0-V reference system.



Note - DLF refers to data line filter (or common-mode choke).

Figure 8. *Moating and Isolation Concept.*

The wafer (or die) internal to the component's assembly is generally located closer to the top of the device package, rather than the bottom, where connection to the I/O pins occur. Height separation from the die to the heat sink is smaller than the height separation between the die and the nearest 0-V reference plane internal to the PCB. Common-mode RF currents generated internal to the package, have no place to couple; hence, RF common-mode currents radiate into free space. Differential-mode decoupling capacitors will not remove common-mode RF energy.

An electrical representation of a typical metal heat sink used for thermodynamic purposes is shown in Figure 10, while Figure 11 shows the implementation of a grounded heat sink design.

A grounded heat sink is always at a 0-V reference potential. The active component (the die within the device package) is at RF voltage po-

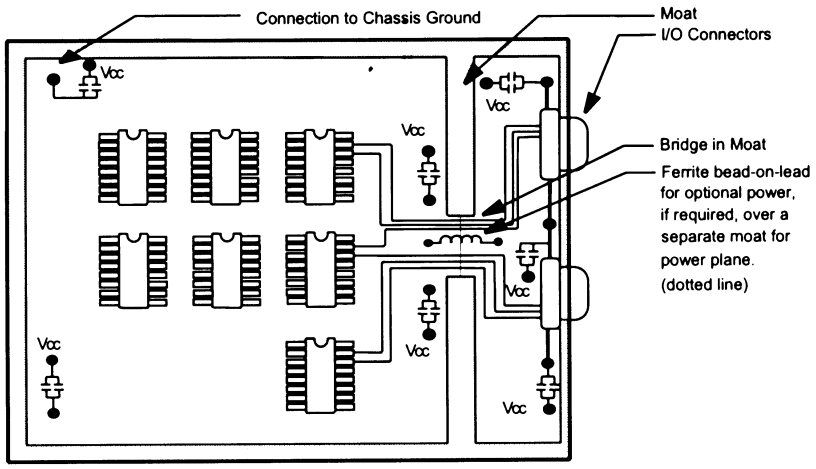
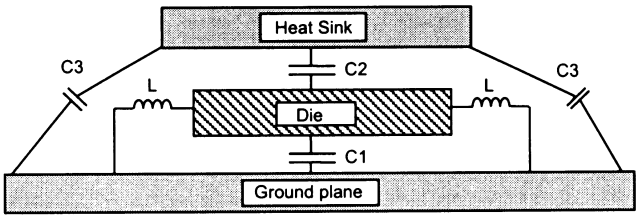


Figure 9. *Proper Use of Bridging a Moat.*



L = Package lead inductance
C1 = Distributed capacitance from the die to the ground plane
C2 = Distributed capacitance from the heat sink to the die
C3 = Distributed capacitance from the heat sink to ground plane or chassis

Typical self-resonant frequency of VLSI processors is approximately 400-800 MHz.

Figure 10. *Electrical Representation of a Metal Heat Sink.*

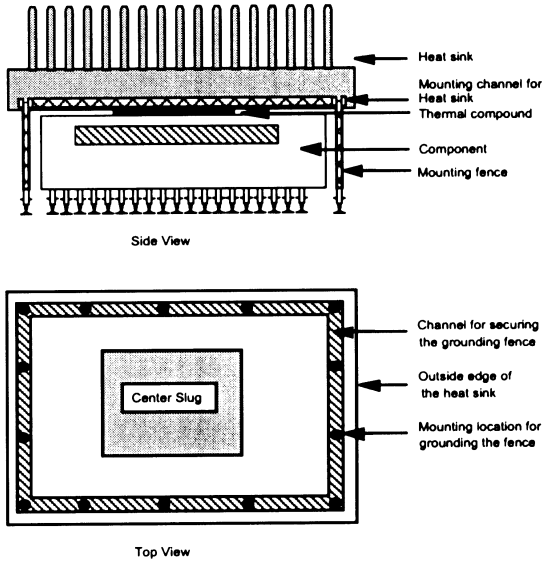


Figure 11. *Implementation of a Grounded Heat Sink.*

tential. The thermal compound between the package and the heat sink is a dielectric material. The definition of a capacitor now exists. Thus, a grounded heat sink works as one large common-mode decoupling capacitor. Discrete capacitors located on the top of the device package, and directly on the PCB, are always provided for differential-mode decoupling. This common-mode decoupling capacitor sinks RF common-mode currents generated *internal* to the processor and sends this current to ground. A common-mode decoupling capacitor will only work if its self-resonant frequency is above the highest frequency of RF energy to be suppressed. The difference between a differential-mode decoupling capacitor and a common-mode heat sink capacitor is that differential-mode capacitors are connected between a power and ground reference source. A common-mode capacitor connects to ground and AC couples RF currents through the dielectric material or thermal compound.

In addition to performing as a common-mode decoupling capacitor, a grounded heat sink acts as a Faraday shield when provided with a properly designed mounting fence which surrounds the component's package completely. This Faraday shield also prevents RF currents created from the clock circuitry within the processor from radiating into free space or coupling to other components or internally-routed cable assemblies.

Conclusion

The important concept of routing traces with periodic signals is to provide a properly-terminated, impedance-controlled signal route adjacent to an RF return image plane. Image planes provide for flux cancellation of RF common-mode currents, and allow the trace to function like a coaxial transmission line. Ground vias allow the RF return path to be undisturbed along the entire trace route if multiple ground planes are provided. Otherwise, a ground trace must be used on the routing plane adjacent to the signal trace to assure a constant, undisturbed RF return path.

Different termination methods are available for traces that have fast edge rates and must travel an electrically long distance within a PCB. For each termination method, there are advantages and disadvantages. The termination method that provides optimal performance for most designs is dependent on what the circuit requires. It is important to remember that if a circuit does not function properly in the time domain, frequency domain concerns are moot.

There are various design and layout techniques available which assist with suppression of RF energy within a PCB. Numerous publications describe concepts, yet few provide simple techniques that can be implemented with minimal effort by both design engineers and PCB designers. Only three techniques are presented herein. There are dozens more. It is the desire of this author to make engineers aware of design concepts and layout techniques, along with how they work, in a format that is easy to understand. These techniques are not generally implemented because they are not obvious when one is only concerned with major details during PCB placement and routing.

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